A1

List of Acronyms Used in the Book and Some Symbols

BJT	Bipolar junction transistor, now commonly used only in small-signal applications.
BNC	A type of circular connector used for coax.
c.m.	Circular mils; 1 c.m. = 5.07×10^{-6} cm^2.
C0G	("cee zero gee") A type of capacitor with essentially zero temperature coefficient.
CAD	Computer-aided design, a common design step in which software is used to lay out traces on a PCB.
CGS	Centimeter-gram-second; one of the standard systems of units.
CM	Common mode; noise current that is in both the power and return lines relative to ground.
DMM	Digital multimeter.
DVM	Digital voltmeter.
EEPROM	Electrically erasable programmable read-only memory.
EMC	Electromagnetic compatibility; ability of two or more systems to work together in the presence of each others' electronic noise.
EMI	Electromagnetic interference; electronic noise causing problems in another system.
EMV	Electromagnetic vulnerability; susceptibility to electronic noise.
ESD	Electrostatic discharge; the little spark you get when shuffling your feet across the carpet.
ESR	Equivalent series resistance (of a capacitor).
FEA	Finite element analysis.
FET	Field effect transistor, see MOSFET.
IGBT	Insulated gate bipolar transistor; the type of power device commonly used in off-line converters.
I_{ib}	Input bias current; the average leakage current into the inverting and noninverting terminals of a comparator or op amp.
I_{ios}	Input offset current; the difference between the leakage currents into the inverting and noninverting terminals of a comparator or op amp.
JFET	Junction field effect transistor (not commonly used in converters).
LED	Light-emitting diode; frequently used for a status display of the health of a converter.
LISN	Line impedance stabilization network; a 50Ω impedance used for EMI measurements.
MKS	Meter-kilogram-second; one of the standard systems of units.
MLC	Multilayer ceramic; a very low ESR capacitor.
MOSFET	Metal oxide semiconductor field effect transistor; the most common power device used in converters.
MOV	Metal oxide varistor; a type of voltage clamping device used for high power transients.
MPP	Molypermalloy powder; a type of magnetic material used for DC inductors.

MTBF	Mean time between failures.
NiCd	Nickel–cadmium; a type of rechargeable cell.
NiH	Nickel–hydrogen, a type of rechargeable cell.
NiMH	Nickel–metal hydride; a type of rechargeable cell.
NM	Normal mode; noise current that flows in the power line relative to return.
NPN	One of the two types of BJT.
NPO	A type of capacitor with essentially zero temperature coefficient.
PCB	Printed circuit board.
PFM	Pulse frequency modulation.
PNP	One of the two types of BJT.
PWM	Pulse width modulation.
$R_{DS,on}$	On resistance, drain to source; the resistance of a fully on MOSFET.
rf	Radio frequency, electromagnetic radiation, used in this book as it pertains to EMI.
RHP(Z)	Right-half-plane (zero); position of a zero that can cause instability in a system.
RMS	Root-mean-square; one method of doing worst-case analysis.
TTL	Transistor–transistor logic; a standard type of logic gate.
UVLO	Under–voltage lockout; a type of circuit that keeps an integrated circuit off until the supply voltage is high enough.
VDE	A standards group in Europe responsible for safety and EMC; also refers to standards from this group.
VRM	Voltage regulation module.
V_f	Forward voltage; the voltage drop from anode to cathode of a diode.
V_{os}	Offset voltage; the equivalent input voltage to a comparator or op amp even when both inputs are tied together.
WCA	Worst-case analysis.

A2

Data Sheets for Worst-Case Analysis

The figures in this Appendix provide the datasheets used to extract parameters for the worst-case analysis of Chapter 10.

COMPUTER DIODE

General Purpose Switching

1N914; JAN, JANTX 1N914
1N4148; JAN, JANTX, JANTXV 1N4148
JAN, JANTX, JANTXV 1N4148-1
1N4531; JAN, JANTX, JANTXV 1N4531

FEATURES

- Metallurgical Bond
- Qualified to MIL-S-19500/116
- Planar Passivated Chip
- DO-34 or DO-35 Package
- Non-JAN Available

DESCRIPTION

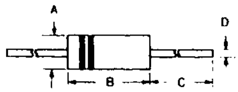
This series is very popular for general purpose switching applications in electronic equipment.

ABSOLUTE MAXIMUM RATINGS, AT 25°C

Reverse Breakdown Voltage		100V
Peak Working Voltage		75V
Average Output Current,	1N914	75mAdc
	1N4148	200mAdc
	1N4148-1	200mAdc
	1N4531	125mAdc
Surge Current, 8.3ms		500mA
Operating Temperature Range		−65°C to +175°C
Storage Temperature Range		−65°C to +200°C

MECHANICAL SPECIFICATIONS

J, JTX 1N914
J, JTX, JTXV 1N4148
J, JTX, JTXV 1N4148-1
J, JTX, JTXV 1N4531



J, JTX & JTXV 1N4531

	INCHES	MILLIMETERS
A	050-.065	1.27-1.65
B	080- 120	2.03-3.05
C	1.0 MIN - 1 5 MAX	25.4 MIN - 38.1 MAX.
D	018-.022	.46- 56

J, JTX 1N914

	INCHES	MILLIMETERS
A	.058-.107	1.42-2.72
B	.140-.300	3 56-7.62
C	1 0 MIN.-1.5 MAX.	25.4 MIN.-38.1 MAX.
D	.018-.022	.46-.56

J, JTX, JTXV 1N4148 and 1N4148-1

	INCHES	MILLIMETERS
A	056- 075	1.42-1 91
B	.140- .180	3 56-4.57
C	1 0 MIN - 1 5 MAX.	25.4 MIN.-38.10 MAX.
D	018-.022	.46-.56

DO-34
1N4531

DO-35
1N914
1N4148

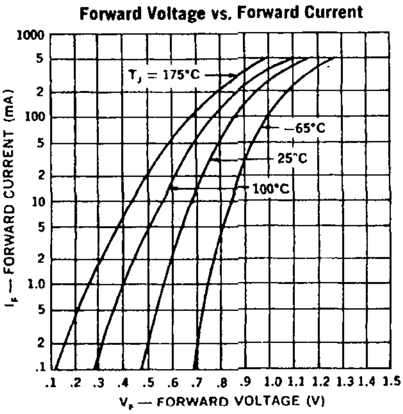
Figure A2.1 Vendor's data sheet for diode 1N4148. (Courtesy of Unitrode Semiconductor Products, Watertown MA.)

1N914; J, JTX 1N914
J, JTX, JTXV 1N4148-1N4148-1
1N4531; J, JTX, JTXV 1N4531

ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Reverse Current @ 25°C	Reverse Current @ 25°C	Peak Reverse Current @ 25°C	Reverse Current @ 150°C	Reverse Current @ 150°C
25nAdc @ $V_R = 20$Vdc	0.5μAdc @ $V_R = 75$Vdc	100μA (pk) @ $V_R = 100$V (pk)	50μAdc @ $V_R = 20$Vdc	100μAdc @ $V_R = 75$Vdc

Forward Voltage	Foward Recovery Voltage	Forward Recovery Time	Reverse Recovery Time	Capacitance
1.0Vdc @ $I_F = 10$mAdc	5.0V (pk) @ $I_F = 50$mAdc	20ns @ $I_F = 50$mAdc	5ns @ $I_F = I_R = 10$mA $R_L = 100$ ohms	4.0 pF @ $V_R = 0$V, f = 1 MHz $V_{sig} = 50$mV (pk-pk) 2.8 pF @ $V_R = 1.5$V, f = 1 MHz $V_{sig} = 50$mV (pk-pk)



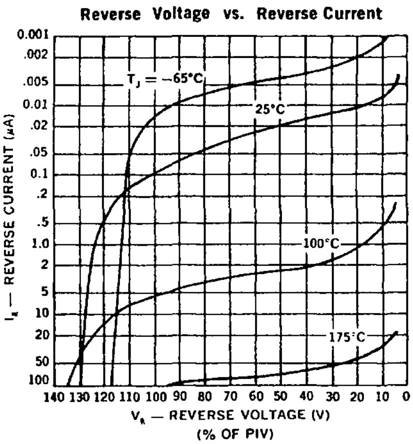
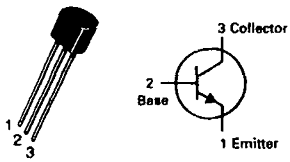


Figure A2.1 (*Continued*)

2N3903
2N3904★

CASE 29-04, STYLE 1
TO-92 (TO-226AA)



GENERAL PURPOSE TRANSISTORS

NPN SILICON

★This is a Motorola designated preferred device.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltge	V_{CBO}	60	Vdc
Emitter-Base Voltage	V_{EBO}	6.0	Vdc
Collector Current — Continuous	I_C	200	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
*Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

***THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W

*Indicates Data in addition to JEDEC Requirements.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) (I_C = 1.0 mAdc, I_B = 0)		$V_{(BR)CEO}$	40	—	Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)		$V_{(BR)CBO}$	60	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)		$V_{(BR)EBO}$	6.0	—	Vdc
Base Cutoff Current (V_{CE} = 30 Vdc, V_{EB} = 3.0 Vdc)		I_{BL}	—	50	nAdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{EB} = 3.0 Vdc)		I_{CEX}	—	50	nAdc
ON CHARACTERISTICS					
DC Current Gain(1) (I_C = 0.1 mAdc, V_{CE} = 1.0 Vdc)	 2N3903 2N3904	h_{FE}	 20 40	 — —	—
(I_C = 1.0 mAdc, V_{CE} = 1.0 Vdc)	2N3903 2N3904		35 70	— —	
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)	2N3903 2N3904		50 100	150 300	
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)	2N3903 2N3904		30 60	— —	
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)	2N3903 2N3904		15 30	— —	
Collector-Emitter Saturation Voltage(1) (I_C = 10 mAdc, I_B = 1.0 mAdc) (I_C = 50 mAdc, I_B = 5.0 mAdc)		$V_{CE(sat)}$	 — —	 0.2 0.3	Vdc
Base-Emitter Saturation Voltage(1) (I_C = 10 mAdc, I_B = 1.0 mAdc) (I_C = 50 mAdc, I_B = 5.0 mAdc)		$V_{BE(sat)}$	 0.65 —	 0.85 0.95	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	 2N3903 2N3904	f_T	 250 300	 — —	MHz

Rev 2

Figure A2.2 Vendor's data sheet for NPN transistor 2N3904. (Copyright of Motorola, used by permission.)

2N3903 2N3904

ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
Output Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz)		C_{obo}	—	4.0	pF
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)		C_{ibo}	—	8.0	pF
Input Impedance (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3903 2N3904	h_{ie}	1.0 1.0	8.0 10	k ohms
Voltage Feedback Ratio (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3903 2N3904	h_{re}	0.1 0.5	5.0 8.0	X 10^{-4}
Small-Signal Current Gain (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3903 2N3904	h_{fe}	50 100	200 400	—
Output Admittance (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{oe}	1.0	40	μmhos
Noise Figure (I_C = 100 μAdc, V_{CE} = 5.0 Vdc, R_S = 1.0 k ohms, f = 1.0 kHz)	2N3903 2N3904	NF	— —	6.0 5.0	dB

SWITCHING CHARACTERISTICS

			Symbol	Min	Max	Unit
Delay Time	(V_{CC} = 3.0 Vdc, V_{BE} = 0.5 Vdc, I_C = 10 mAdc, I_{B1} = 1.0 mAdc)		t_d	—	35	ns
Rise Time			t_r	—	35	ns
Storage Time	(V_{CC} = 3.0 Vdc, I_C = 10 mAdc, I_{B1} = I_{B2} = 1.0 mAdc)	2N3903 2N3904	t_s	— —	175 200	ns
Fall Time			t_f	—	50	ns

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 – DELAY AND RISE TIME EQUIVALENT TEST CIRCUIT

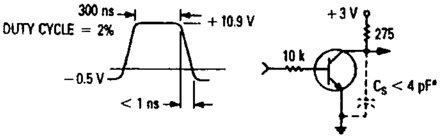
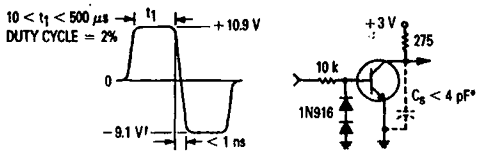


FIGURE 2 – STORAGE AND FALL TIME EQUIVALENT TEST CIRCUIT



*Total shunt capacitance of test jig and connectors

TYPICAL TRANSIENT CHARACTERISTICS

— T_J = 25°C - - - T_J = 125°C

FIGURE 3 – CAPACITANCE

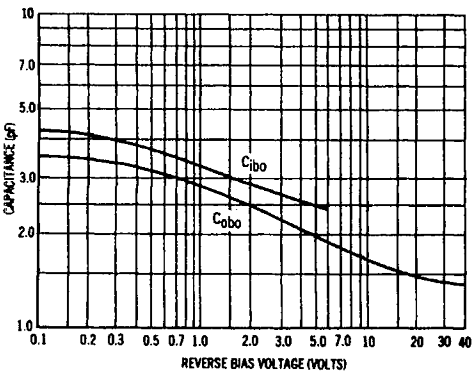


FIGURE 4 – CHARGE DATA

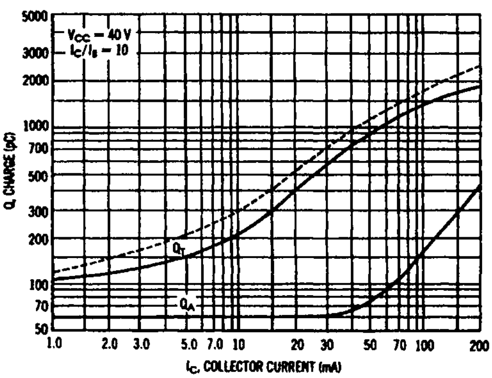


Figure A2.2 *(Continued)*

2N3903 2N3904

FIGURE 5 – TURN-ON TIME

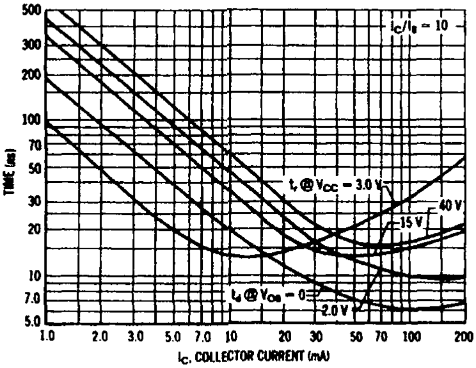


FIGURE 6 – RISE TIME

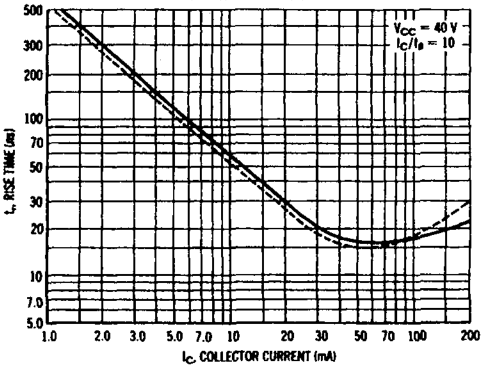


FIGURE 7 – STORAGE TIME

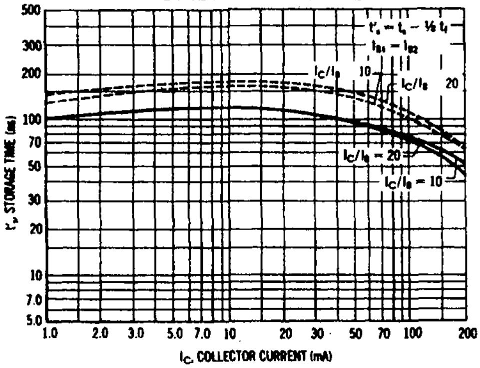
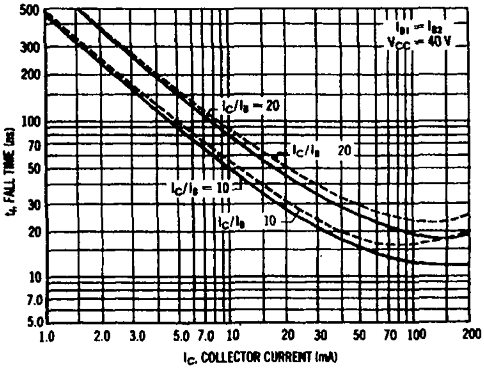


FIGURE 8 – FALL TIME



TYPICAL AUDIO SMALL-SIGNAL CHARACTERISTICS

NOISE FIGURE VARIATIONS

$V_{CE} = 5.0$ Vdc, $T_A = 25°C$,
Bandwidth = 1.0 Hz

FIGURE 9

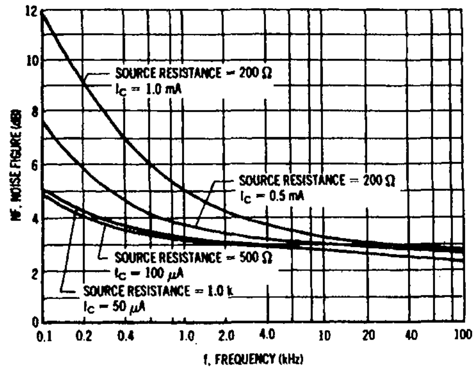


FIGURE 10

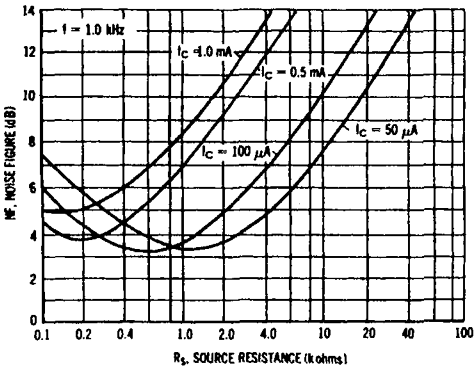


Figure A2.2 (*Continued*)

2N3903 2N3904

h PARAMETERS

(V_{CE} = 10 Vdc, f = 1.0 kHz, T_A = 25°C)

FIGURE 11 – CURRENT GAIN

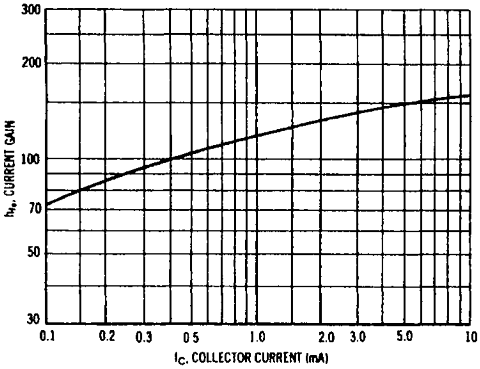


FIGURE 12 – OUTPUT ADMITTANCE

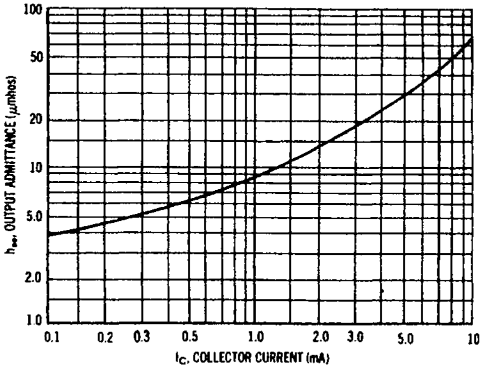


FIGURE 13 – INPUT IMPEDANCE

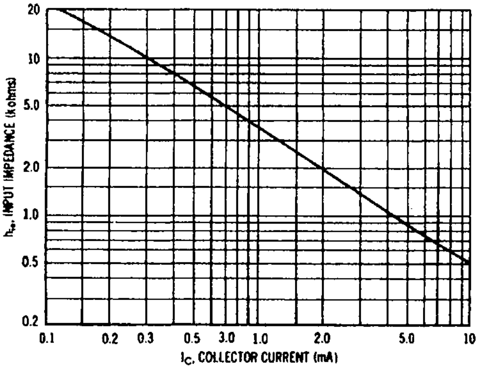
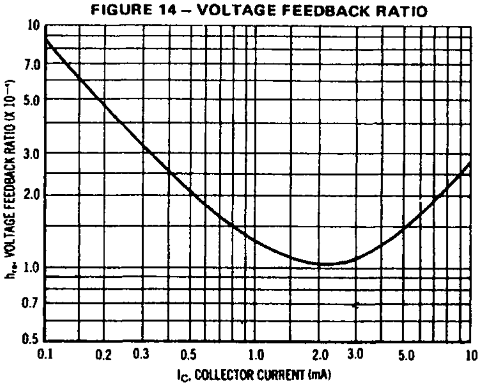


FIGURE 14 – VOLTAGE FEEDBACK RATIO



TYPICAL STATIC CHARACTERISTICS

FIGURE 15 – DC CURRENT GAIN

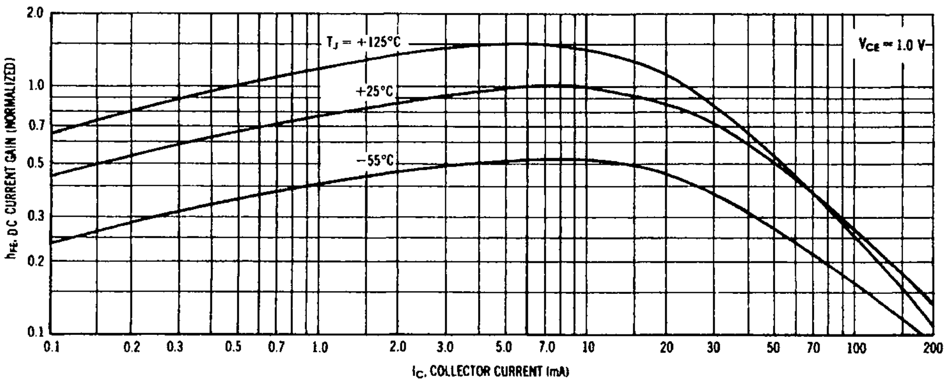


Figure A2.2 (*Continued*)

2N3903 2N3904

FIGURE 16 – COLLECTOR SATURATION REGION

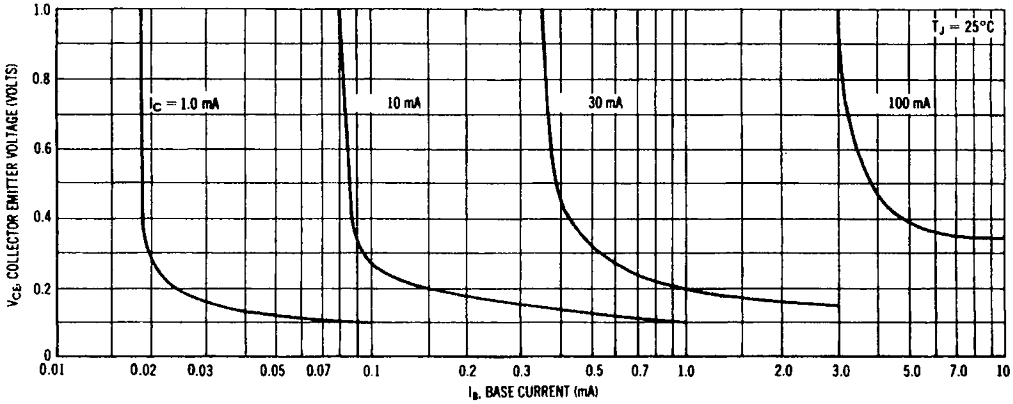


FIGURE 17 – "ON" VOLTAGES

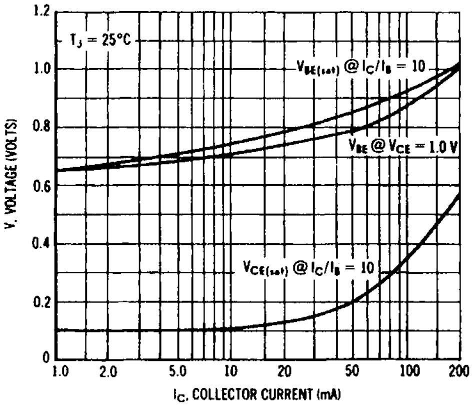


FIGURE 18 – TEMPERATURE COEFFICIENTS

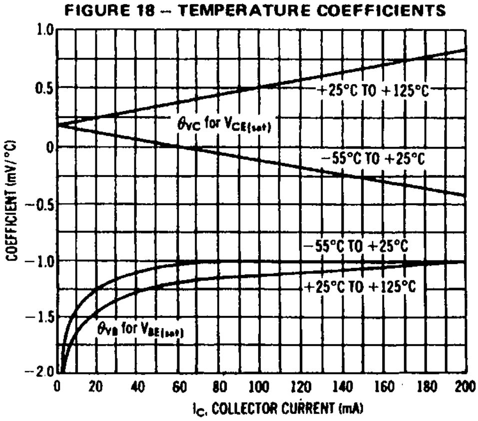


Figure A2.2 (*Continued*)

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

LM139,A
LM239,A, LM2901,
LM339,A, MC3302

Quad Single Supply Comparators

These comparators are designed for use in level detection, low-level sensing and memory applications in consumer automotive and industrial electronic applications.

- Single or Split Supply Operation
- Low Input Bias Current: 25 nA (Typ)
- Low Input Offset Current: ±5.0 nA (Typ)
- Low Input Offset Voltage: ±1.0 mV (Typ) LM139A Series
- Input Common Mode Voltage Range to Gnd
- Low Output Saturation Voltage: 130 mV (Typ) @ 4.0 mA
- TTL and CMOS Compatible
- ESD Clamps on the Inputs Increase Reliability without Affecting Device Operation

QUAD COMPARATORS

SILICON MONOLITHIC INTEGRATED CIRCUIT

N, P SUFFIX
PLASTIC PACKAGE
CASE 646

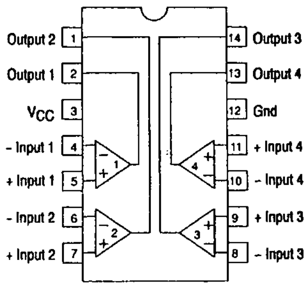
J, L SUFFIX
CERAMIC PACKAGE
CASE 632

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

MAXIMUM RATINGS

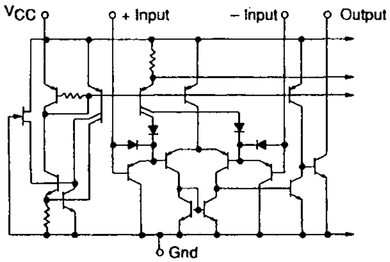
Rating	Symbol	Value	Unit
Power Supply Voltage LM139, A/LM239, A/LM339A/LM2901 MC3302	V_{CC}	 +36 or ±18 +30 or ±15	Vdc
Input Differential Voltage Range LM139, A/LM239, A/LM339, A/LM2901 MC3302	V_{IDR}	 36 30	Vdc
Input Common Mode Voltage Range	V_{ICMR}	–0.3 to V_{CC}	Vdc
Output Short Circuit to Ground (Note 1)	I_{SC}	Continuous	
Input Current (V_{in} < – 0.3 Vdc) (Note 2)	I_{in}	50	mA
Power Dissipation @ T_A = 25°C Ceramic Plastic Package Derate above 25°C	P_D	 1.0 8.0	 W mW/°C
Junction Temperature Ceramic & Metal Package Plastic Package	T_J	 175 150	°C
Operating Ambient Temperature Range LM139, A LM239, A MC3302 LM2901 LM339, A	T_A	 –55 to +125 –25 to +85 –40 to +85 –40 to +105 0 to +70	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

PIN CONNECTIONS



(Top View)

Figure 1. Circuit Schematic



NOTE: Diagram shown is for 1 comparator.

ORDERING INFORMATION

Device	Temperature Range	Package
LM139J, AJ	–55° to +125°C	Ceramic DIP
LM239D, AD LM239J, AJ LM239N, AN	–25° to +85°C	SO-14 Ceramic DIP Plastic DIP
LM339D, AD LM339J, AJ LM339N, AN	0° to +70°C	SO-14 Ceramic DIP Plastic DIP
LM2901D LM2901N	–40° to +105°C	SO-14 Plastic DIP
MC3302L MC3302P	–40° to +85°C	Ceramic DIP Plastic DIP

Figure A2.3 Vendor's data sheet for Quad Comparator LM139. (Copyright of Motorola, used by permission.)

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, T_A = +25°C, unless otherwise noted)

Characteristics	Symbol	LM139A			LM239A/339A			LM139			LM239/339			LM2901			MC3302			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 4)	V_{IO}	—	±1.0	±2.0	—	±1.0	±2.0	—	±2.0	±5.0	—	±2.0	±5.0	—	±2.0	±7.0	—	±3.0	±20	mVdc
Input Bias Current (Notes 4, 5) (Output in Linear Range)	I_{IB}	—	25	100	—	25	250	—	25	100	—	25	250	—	25	250	—	25	500	nA
Input Offset Current (Note 4)	I_{IO}	—	±3.0	±25	—	±5.0	±50	—	±3.0	±25	—	±5.0	±50	—	±5.0	±50	—	±3.0	±100	nA
Input Common Mode Voltage Range	V_{ICMR}	0	—	V_{CC} −1.5	0	—	V_{CC} −1.5	0	—	V_{CC} −1.5	0	—	V_{CC} −1.5	0	—	V_{CC} −1.5	0	—	V_{CC} −1.5	V
Supply Current R_L = ∞ (For All Comparators) R_L = ∞, V_{CC} = 30 Vdc	I_{CC}	— —	0.8 1.0	2.0 2.5	— —	0.8 1.0	2.0 2.5	— —	0.8 1.0	2.0 2.5	— —	0.8 1.0	2.0 2.5	— —	0.8 1.0	2.0 2.5	— —	0.8 1.0	2.0 2.5	mA
Voltage Gain R_L ≥ 15 kΩ, V_{CC} = 15 Vdc	A_{VOL}	50	200	—	50	200	—	—	200	—	—	200	—	25	100	—	2	30	—	V/mV
Large Signal Response Time V_I = TTL Logic Swing, V_{ref} = 1.4 Vdc, V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ	—	—	300	—	—	300	—	—	300	—	—	300	—	—	300	—	—	300	—	ns
Response Time (Note 6) V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ	—	—	1.3	—	—	1.3	—	—	1.3	—	—	1.3	—	—	1.3	—	—	1.3	—	µs
Output Sink Current V_I(−) ≥ +1.0 Vdc, V_I(+) = 0, V_O ≤ 1.5 Vdc	I_{Sink}	6.0	16	—	6.0	16	—	6.0	16	—	6.0	16	—	6.0	16	—	6.0	16	—	mA
Saturation Voltage V_I(−) ≥ +1.0 Vdc, V_I(+) = 0, I_{sink} ≤ 4.0 mA	V_{sat}	—	130	400	—	130	400	—	130	400	—	130	400	—	130	400	—	130	500	mV
Output Leakage Current V_I(+) ≥ +1.0 Vdc, V_I(−) = 0, V_O = +5.0 Vdc	I_{OL}	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	—	nA

PERFORMANCE CHARACTERISTICS (V_{CC} = +5.0 Vdc, T_A = T_{low} to T_{high} [Note 3])

Characteristics	Symbol	LM139A			LM239A/339A			LM139			LM239/339			LM2901			MC3302			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 4)	V_{IO}	—	—	±4.0	—	—	±4.0	—	—	±9.0	—	—	±9.0	—	—	±15	—	—	±40	mVdc
Input Bias Current (Notes 4, 5) (Output in Linear Range)	I_{IB}	—	—	300	—	—	400	—	—	300	—	—	400	—	—	500	—	—	1000	nA
Input Offset Current (Note 4)	I_{IO}	—	—	±100	—	—	±150	—	—	±100	—	—	±150	—	—	±200	—	—	±300	nA
Input Common Mode Voltage Range	V_{ICMR}	0	—	V_{CC} −2.0	0	—	V_{CC} −2.0	0	—	V_{CC} −2.0	0	—	V_{CC} −2.0	0	—	V_{CC} −2.0	0	—	V_{CC} −2.0	V
Saturation Voltage V_I(−) ≥ +1.0 Vdc, V_I(+) = 0, I_{sink} ≤ 4.0 mA	V_{sat}	—	—	700	—	—	700	—	—	700	—	—	700	—	—	700	—	—	700	mV
Output Leakage Current V_I(+) ≥ +1.0 Vdc, V_I(−) = 0, V_O = 30 Vdc	I_{OL}	—	—	1.0	—	—	1.0	—	—	1.0	—	—	1.0	—	—	1.0	—	—	1.0	µA
Differential Input Voltage All V_I ≥ 0 Vdc	V_{ID}	—	—	V_{CC}	—	—	V_{CC}	—	—	V_{CC}	—	—	V_{CC}	—	—	V_{CC}	—	—	V_{CC}	Vdc

NOTES:

1. The maximum output current may be as high as 20 mA, independent of the magnitude of V_{CC}. Output short circuits to V_{CC} can cause excessive heating and eventual destruction.
2. This magnitude of input current will only occur if the leads are driven more negative than ground or the negative supply voltage. This is due to the input PNP collectorbase junction becoming forward biased, acting as an input clamp diode. There is also a lateral PNP parasitic transistor action which can cause the output voltage of the comparators to go to the V_{CC} voltage level (or ground if overdrive is large) during the time that an input is driven negative. This will not destroy the device when limited to the max rating and normal output states will recover when the inputs become ≥ ground or negative supply.
3. (LM139/139A) T_{low} = −55°C, T_{high} = +125°C; (LM239/239A) T_{low} = −25°C, T_{high} = +85°C; (LM339/339A) T_{low} = 0°C, T_{high} = +70°C; (MC3302) T_{low} = −40°C, T_{high} = +85°C; (LM2901) T_{low} = −40°C, T_{high} = +105°C
4. At the output switch point, V_O ≃ 1.4 Vdc, R_S ≤ 100 Ω 5.0 Vdc ≤ V_{CC} ≤ 30 Vdc, with the inputs over the full common mode range (0 Vdc to V_{CC} −1.5 Vdc).
5. The bias current flows out of the inputs due to the PNP input stage. This current is virtually constant, independent of the output state.
6. The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger signals, 300 ns is typical.

Figure A2.3 *(Continued)*

LM139,A, LM239,A, LM339,A, LM2901, MC3302

Typical Characteristics

(V_{CC} = 1.5 Vdc, T_A = +25°C (each comparator) unless otherwise noted.)

Figure 4. Normalized Input Offset Voltage

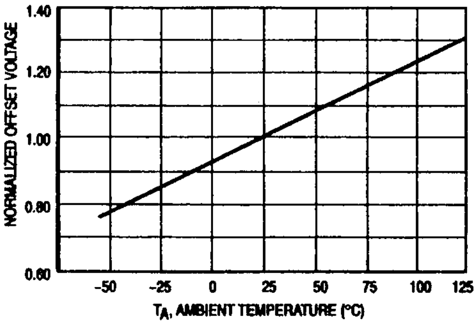


Figure 5. Input Bias Current

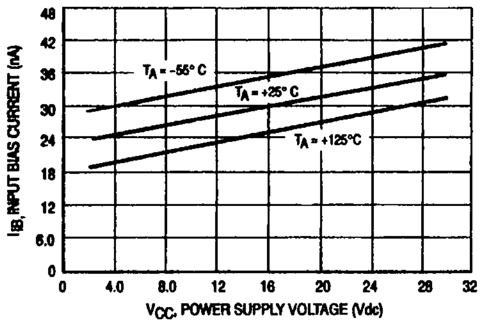


Figure 6. Output Sink Current versus Output Saturation Voltage

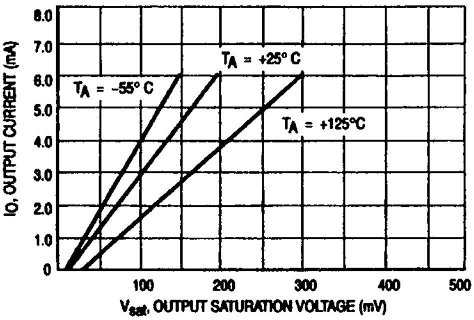


Figure A2.3 *(Continued)*

UC1825
UC2825
UC3825

High Speed PWM Controller

FEATURES

- Compatible with Voltage or Current Mode Topologies
- Practical Operation Switching Frequencies to 1MHz
- 50ns Propagation Delay to Output
- High Current Dual Totem Pole Outputs (1.5A Peak)
- Wide Bandwidth Error Amplifier
- Fully Latched Logic with Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Soft Start / Max. Duty Cycle Control
- Under-Voltage Lockout with Hysteresis
- Low Start Up Current (1.1mA)
- Trimmed Bandgap Reference (5.1V ±1%)

DESCRIPTION

The UC1825 family of PWM control ICs is optimized for high frequency switched mode power supply applications. Particular care was given to minimizing propagation delays through the comparators and logic circuitry while maximizing bandwidth and slew rate of the error amplifier. This controller is designed for use in either current-mode or voltage mode systems with the capability for input voltage feed-forward.

Protection circuitry includes a current limit comparator with a 1V threshold, a TTL compatible shutdown port, and a soft start pin which will double as a maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at an output. An under-voltage lockout section with 800mV of hysteresis assures low start up current. During under-voltage lockout, the outputs are high impedance.

These devices feature totem pole outputs designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The on state is designed as a high level.

BLOCK DIAGRAM

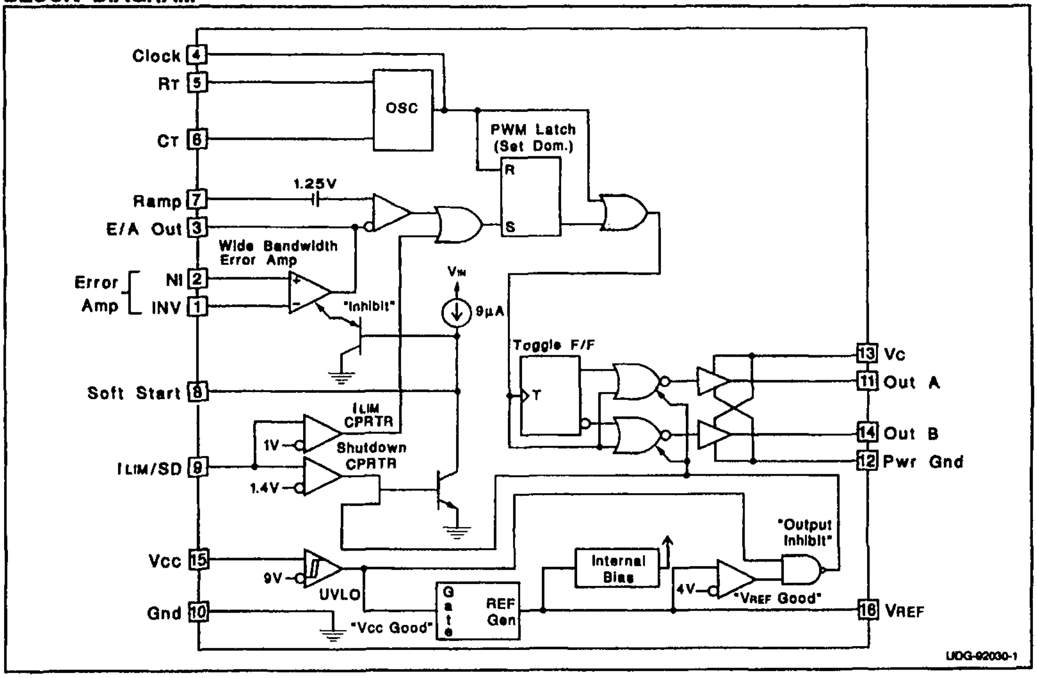


Figure A2.4 Vendor's data sheet for PWM controller UC2825. (Courtesy of Unitrode Semiconductor Products, Watertown MA.)

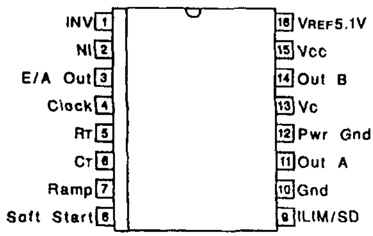
UC3825

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Pins 13, 15) 30V
Output Current, Source or Sink (Pins 11, 14)
DC. 0.5A
Pulse (0.5ms) 2.0A
Analog Inputs
(Pins 1, 2, 7) . . . . -0.3V to 7V
(Pin 8, 9) . . . . -0.3V to 6V
Clock Output Current (Pin 4) . . . . -5mA
Error Amplifier Output Current (Pin 3) 5mA
Soft Start Sink Current (Pin 8) 20mA
Oscillator Charging Current (Pin 5) . . . . -5mA
Power Dissipation 1W
Storage Temperature Range . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) . . . . 300°C

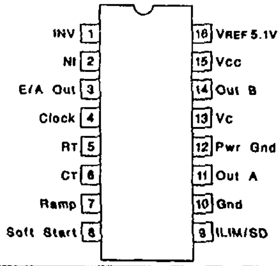
Note 1: All voltages are with respect to GND (Pin 10); all currents are positive into, negative out of part; pin numbers refer to DIL-16 package.
Note 3: Consult Unitrode Integrated Circuit Databook for thermal limitations and considerations of package.

SOIC-16 (Top View)
DW Package

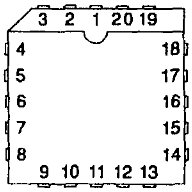


CONNECTION DIAGRAMS

DIL-16 (Top View)
J Or N Package



PLCC-20 & LCC-20
(Top View)
Q & L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
INV	2
NI	3
E/A Out	4
Clock	5
N/C	6
RT	7
CT	8
Ramp	9
Soft Start	10
N/C	11
ILIM/SD	12
Gnd	13
Out A	14
Pwr Gnd	15
N/C	16
Vc	17
Out B	18
Vcc	19
VREF 5.1V	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated,these specifications apply for , RT = 3.65k, CT = 1nF, Vcc = 15V, -55°C<TA<125°C for the UC1825, –40°C<TA<85°C for the UC2825, and 0°C<TA<70°C for the UC3825, TA=TJ.

PARAMETERS	TEST CONDITIONS	UC1825 UC2825			UC3825			
		MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Reference Section								
Output Voltage	TJ = 25°C, Io = 1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	10V < Vcc < 30V		2	20		2	20	mV
Load Regulation	1mA < Io < 10mA		5	20		5	20	mV
Temperature Stability*	TMIN < TA < TMAX		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation*	Line, Load, Temperature	5.00		5.20	4.95		5.25	V
Output Noise Voltage*	10Hz < f < 10kHz		50			50		µV
Long Term Stability*	TJ = 125°C, 1000hrs.		5	25		5	25	mV
Short Circuit Current	VREF = 0V	-15	-50	-100	-15	-50	-100	mA
Oscillator Section								
Initial Accuracy*	TJ = 25°C	360	400	440	360	400	440	kHz
Voltage Stability*	10V < Vcc < 30V		0.2	2		0.2	2	%
Temperature Stability*	TMIN < TA < TMAX		5			5		%
Total Variation*	Line, Temperature	340		460	340		460	kHz

Figure A2.4 *(Continued)*

UC1825
UC2825
UC3825

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated,these specifications apply for , R_T = 3.65k, C_T = 1nF, V_{CC} = 15V, -55°C<T_A<125°C for the UC1825, –40°C<T_A<85°C for the UC2825, and 0°C<T_A<70°C for the UC3825, T_A=T_J.

PARAMETERS	TEST CONDITIONS	UC1825 UC2825			UC3825			
		MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Oscillator Section (cont)								
Clock Out High		3.9	4.5		3.9	4.5		V
Clock Out Low			2.3	2.9		2.3	2.9	V
Ramp Peak*		2.6	2.8	3.0	2.6	2.8	3.0	V
Ramp Valley*		0.7	1.0	1.25	0.7	1.0	1.25	V
Ramp Valley to Peak*		1.6	1.8	2.0	1.6	1.8	2.0	V
Error Amplifier Section								
Input Offset Voltage				10			15	mV
Input Bias Current			0.6	3		0.6	3	µA
Input Offset Current			0.1	1		0.1	1	µA
Open Loop Gain	1V < Vo < 4V	60	95		60	95		dB
CMRR	1.5V < V_{CM} < 5.5V	75	95		75	95		dB
PSRR	10V < V_{CC} < 30V	85	110		85	110		dB
Output Sink Current	$V_{PIN\,3}$ = 1V	1	2.5		1	2.5		mA
Output Source Current	$V_{PIN\,3}$ = 4V	-0.5	-1.3		-0.5	-1.3		mA
Output High Voltage	$I_{PIN\,3}$ = -0.5mA	4.0	4.7	5.0	4.0	4.7	5.0	V
Output Low Voltage	$I_{PIN\,3}$ = 1mA	0	0 .5	1.0	0	0.5	1.0	V
Unity Gain Bandwidth*		3	5.5		3	5.5		MHz
Slew Rate*		6	12		6	12		V/µs
PWM Comparator Section								
Pin 7 Bias Current	$V_{PIN\,7}$ = 0V		-1	-5		-1	-5	µA
Duty Cycle Range		0		80	0		85	%
Pin 3 Zero DC Threshold	$V_{PIN\,7}$ = 0V	1.1	1.25		1.1	1.25		V
Delay to Output*			50	80		50	80	ns
Soft Start Section								
Charge Current	$V_{PIN\,8}$ = 0.5V	3	9	20	3	9	20	µA
Discharge Current	$V_{PIN\,8}$ = 1V	1			1			mA
Current Limit / Shutdown Section								
Pin 9 Bias Current	0 < $V_{PIN\,9}$ < 4V			15			10	µA
Current Limit Threshold		0.9	1.0	1.1	0.9	1.0	1.1	V
Shutdown Threshold		1.25	1.40	1.55	1.25	1.40	1.55	V
Delay to Output			50	80		50	80	ns
Output Section								
Output Low Level	I_{OUT} = 20mA		0.25	0.40		0.25	0.40	V
	I_{OUT} = 200mA		1.2	2.2		1.2	2.2	V
Output High Level	I_{OUT} = -20mA	13.0	13.5		13.0	13.5		V
	I_{OUT} = -200mA	12.0	13.0		12.0	13.0		V
Collector Leakage	V_C = 30V		100	500		10	500	µA
Rise/Fall Time*	CL = 1nF		30	60		30	60	ns
Under-Voltage Lockout Section								
Start Threshold		8.8	9.2	9.6	8.8	9.2	9.6	V
UVLO Hysteresis		0.4	0.8	1.2	0.4	0.8	1.2	V
Supply Current Section								
Start Up Current	V_{CC} = 8V		1.1	2.5		1.1	2.5	mA
ICC	$V_{PIN\,1}$, $V_{PIN\,7}$, $V_{PIN\,9}$ = 0V; $V_{PIN\,2}$ = 1V		22	33		22	33	mA

** This parameter not 100% tested in production but guaranteed by design.*

Figure A2.4 (*Continued*)

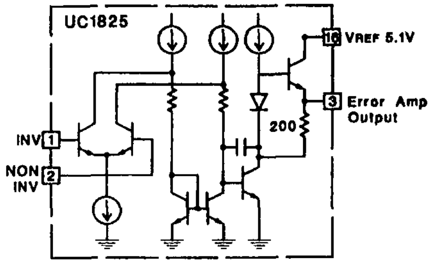
UC1825
UC2825
UC3825

Printed Circuit Board Layout Considerations

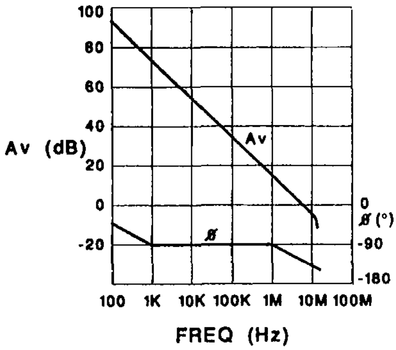
High speed circuits demand careful attention to layout and component placement. To assure proper performance of the UC1825 follow these rules: 1) Use a ground plane. 2) Damp or clamp parasitic inductive kick energy from the gate of driven MOSFETs. Do not allow the output pins to ring below ground. A series gate resistor or a shunt 1 Amp Schottky diode at the output pin will serve this purpose. 3) Bypass Vcc, Vc, and VREF. Use 0.1μF monolithic ceramic capacitors with low equivalent series inductance. Allow less than 1 cm of total lead length for each capacitor between the bypassed pin and the ground plane. 4) Treat the timing capacitor, CT, like a bypass capacitor.

Error Amplifier Circuit

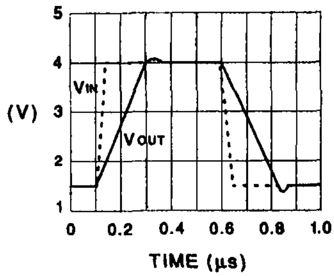
Simplified Schematic



Open Loop Frequency Response

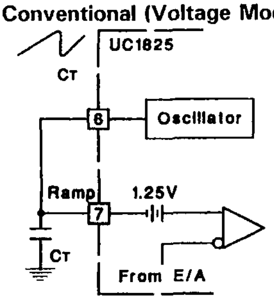


Unity Gain Slew Rate

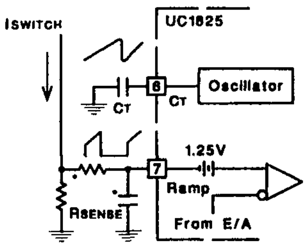


PWM Applications

Conventional (Voltage Mode)



Current Mode



* A small filter may be required to suppress switch noise.

Figure A2.4 (*Continued*)

UC1825
UC2825
UC3825

Oscillator Circuit

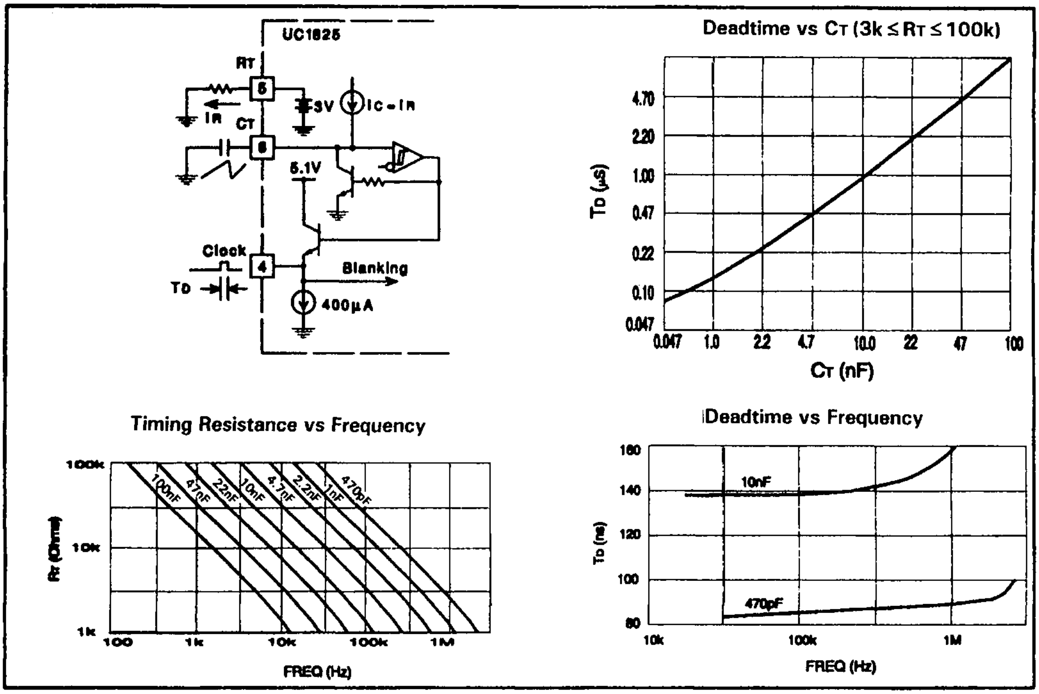


Figure A2.4 (*Continued*)

Output Section

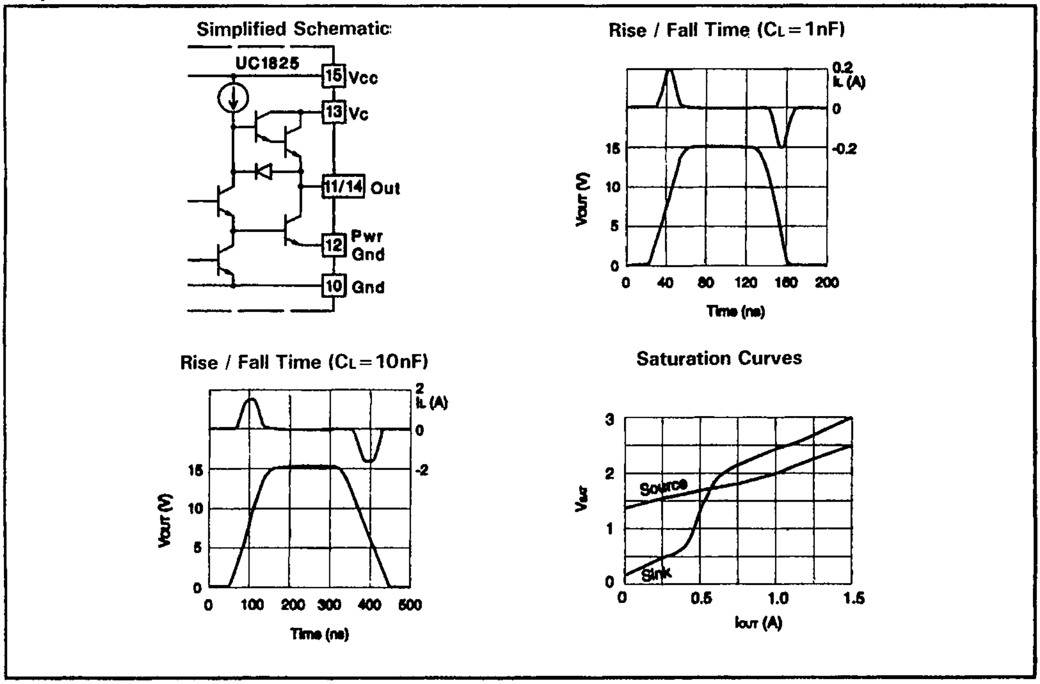


Figure A2.4 (*Continued*)