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Practical Worst-Case Analysis

INTRODUCTION

The Purpose of Worst-Case Analysis

If all you had to do was build a single supply that would operate on your lab bench for a couple of hours, you could get a system running and forget it. In reality, of course, your breadboard is a prototype for hundreds or thousands or even millions of supplies, every one of which ideally would operate over a range of temperatures and power sources and loads, would meet the specifications regardless of component tolerances, and would continue doing so for many years. The purpose of worst-case analysis (WCA) is to ensure that your design is robust—that is, even if all the varying conditions mentioned above occur in a single supply, the supply would operate within specifications over its lifetime.

Given this statement of purpose, it is obvious that WCA is an essential step in design, and time and budget must be allocated for each design that is intended to reach production. Since this step is often ignored, it purpose must be explained to management, and it must be repeatedly stressed to management that WCA is *essential* for creating a reliable product.

How Do You Do WCA?

The general idea of WCA is to take each and every component of the design, find its worst possible value(s) for the function or functions it is intended to perform, and verify, either mathematically or through simulations, that the function is correctly performed even when all these worst-case values occur simultaneously. "Mathematically" here refers to some combination of analytical solutions and numerical approximation; "analytical" means real, old-fashioned algebra (calculus, differential equations, etc.); simulations are tests of operation using a computer model, but *not* Monte Carlo methods, for reasons explained

below. The preferred method is analytical because it *proves* what you are trying to show; numerical work is next in line, with simulation being the least desirable. The problem with simulations, as discussed below, is not that the computer might make a mistake (although this has been known to happen!), but rather that you are at the mercy of whoever wrote the simulation software, and whoever made the simulation models; if the model wasn't tested the way you use it, there's no way of telling whether its results are valid for your application, and typically the model is unavailable to the person doing the simulation.

The author has developed a systematic method for doing WCA that reduces what is at first blush an overwhelming task into a manageable, if somewhat tedious set of procedures. Indeed, once you have done WCA a few times, you'll notice that many of the circuits you analyze repeat themselves from design to design, and so the analyses done for the one supply apply to the next. Eventually you learn to *design* things in such a way that they will pass WCA.

The first step is natural. Simply break up the circuit into function blocks: this block is a timer, this block is overcurrent shutdown, etc. Each block is then going to be the subject of its own WCA. Of course there will be some inputs from other blocks, but since you're going to be doing a WCA on the other blocks also, you can assume that those other blocks meet the spec requirements.

Having identified a block, the next step is to assemble a table indicating the maximum and minimum value of each (relevant) parameter of each component. Of course, you can't know exactly which parameters are going to be needed up front, but with some experience you can make some good guesses. (See the example below for details on table entries.) Other parameters can be calculated and entered into the table as the work progresses.

The first page of a WCA is an overall description of the function of the circuit block, stating the conditions of operation, listing each parameter that is to be analyzed, and providing a conclusion that the block works as it's supposed to (the presumption being that the design is changed until it *does* work—WCA will make it clear which components need to be changed). The following pages constitute the analyses of each parameter, preferably organized as one analysis per document to make revision easy; then there is a page showing a stress analysis (see below); and the last page is the completed parameter table. This then constitutes a complete analysis of the function block, which can be assembled with other such analyses to form a book documenting the validity of the power supply design.

When doing the analysis, don't forget that some circuits may have their worst case during start-up rather than during steady-state operation. Many converter designs have been known to fail exclusively at start-up!

The Purpose of Stress Analysis

Just to be clear, a stress analysis is different from a worst-case analysis. The purpose of a WCA is to determine that the circuitry functions according to specification; the purpose of a stress analysis is to verify that none of the components is exceeding its ratings (or derating guidelines).

Whether you use the manufacturer's ratings for the stress analysis (after all, they have some margins built into their specs, too) or one of the common derating guidelines (the author typically uses military derating guidelines) is of course a matter of company

policy. It is something you have to know up front, however. Be sure to find out before getting started. You don't want to do these analyses repeatedly if you can possibly avoid it!

RMS versus Worst Case

Some readers may have noticed a certain vagueness in the statement of exactly what a WCA is going to analyze. Does the statement that the correct functioning of the circuit must be established in the case that all the components and conditions are at their worst value mean that everything is "worst" *simultaneously* and *on the same unit*? The usual argument against this interpretation (which the author refers to as "worst-case") is that it is impossibly rare for all the worst conditions and components to conspire in such a way as to all end up on a single supply. Given this presumption, it is argued, it is more reasonable to do an "RMS" analysis, in which the effect of each component going to its worst-case value is orthogonal to the effect of every other component. For example, if the effect of a worst-case value of R_1 is to increase some condition's value by 10%, and the effect of a worst-case value of R_2 is also to increase the same condition's value by 10%, the effect in RMS is only $(1.10^2 + 1.10^2)^{1/2} = 1.14 = 14\%$ versus $1.10 \times 1.10 = 1.21 = 21\%$ in worst-case.

> **Practical Note** You spare yourself little effort by doing RMS instead of worst-case WCA. There is usually not much circuitry difference either. The practical approach is to use worst-case unless you're sure that so few units will be built that statistics won't be too important. So for everything except small runs of manufacturing (say 100 pieces or less), it makes sense to go ahead and verify the circuitry with worst-case rather than RMS WCA. Of course, for small runs of critical designs (e.g., on a satellite), worst-case needs to be done instead of RMS. In any case, make sure your management understands the issue and has made a decision regarding the appropriate goal before you get started.

Mathematics versus Simulation

Here is a tempting possibility: throw the whole circuit on the computer, and let *it* figure out the answer, instead of you hurting your head. You'll see in the example below that the author never does this (with one exception, noted in the next paragraph). The reason is that a user just doesn't know whether the authors of the simulation's model were thorough enough to capture all the parameters of interest to the analysis at hand. Of course the device works like a comparator, but does it correctly model input bias current? Input offset voltage with temperature? Output saturation voltage with current and temperature and die lot variations? The author once found a simulation model, in an expensive simulation program, of an open collector comparator whose output would go to +15V without a pull-up resistor! Your lack of knowledge about the model makes relying on a simulation a bad idea.

There is a single exception to the foregoing proscription against use of a computer for WCA, however: determining phase margin of a converter is so complicated that you really don't want to do it by hand (although it *could* be done with a symbolic mathematics program). Fortunately, all the important parameters (inductance and resistance of the

inductor, capacitance and ESR of the output cap, etc.) can be entered into the computer directly; you don't have to rely on models. The only IC parameters of interest are the open loop gain of the error amp and the ramp amplitude of the PWM. So WCA of phase margin can be safely done by computer, simply varying each component individually to see whether it should be a maximum or minimum to get minimum phase margin, and then setting all the components to their respective minima or maxima simultaneously (at least for a minimum-phase system).

Monte Carlo? Sensitivity Analysis?

Monte Carlo analysis goes computer-based WCA one step worse: it not only relies on models of unknown validity, it also implicitly assumes something akin to RMS analysis. The trouble is in the great number of cases you need to simulate to get a certain level of confidence that a parameter is OK.

EXAMPLE

We need to be 99% certain that six parameters varying simultaneously won't cause a problem in some circuitry. How many Monte Carlo analyses do we need? If you guessed something like $2^6 = 64$, you're way off. Let's assume that the probabilities are lumped at the two ends—that is, each parameter is either a minimum or a maximum (a bimodal distribution). There are thus a total of $2^6 = 64$ possible value sets (i.e., component 1 is low, 2 is high, etc., constitutes a single value set). Each time you do an analysis you get one of these 64, so your chances of hitting the worst one are 1 in 64 each time. The chances of not getting it are clearly one minus this, $1 - (1/64)$. The chances of not hitting the worst one after N trials is $[1 - (1/64)]^N$, and this number has to equal $1 - 99\% = 0.01$. We have

$$\left(1 - \frac{1}{64}\right)^N = 0.01$$

which yields $N = 292$! And clearly this number gets larger very fast, as either the number of parameters grows or the certainty required grows. And since the end result is that even after 292 trials you're *still* not certain (you can't be sure that you got the worst case no matter how many trials you made), it just isn't a good idea to do WCA with Monte Carlo analysis.

As for sensitivity analysis, again you don't know whether the computer has the right models. This mode of analysis may be useful for knowing which parameters to concentrate most attention on, but ultimately, you still need to look at them all, because otherwise you won't know what level of sensitivity is low enough to be ignored. It is also to be observed that sensitivity analysis is a linearization of the models around a particular operating point—if the operating point varies, the results of the sensitivity analysis do too.

AN EXHAUSTING EXAMPLE

The purpose of this section is to give a sample WCA of a common circuit block in full detail. This will then serve as a template for the reader to do his or her own analyses. Take the time to read this example through carefully; there are many helpful techniques to be gleaned from it. The author feels confident that after reading through this detailed

example, you will be in agreement with the title of this section, but you will be ready to analyze your own circuits.

The Circuit

The circuit block to be analyzed (see Figure 10.1) can be described fairly simply and is pretty common in practice. When a comparator that is sensing some function (let's say the current from a low impedance resistor) detects that this current has gone too high, it turns on a BJT that discharges a cap; the cap is attached to the soft-start pin on a PWM IC, in this case a UC3825, and turns the IC off.

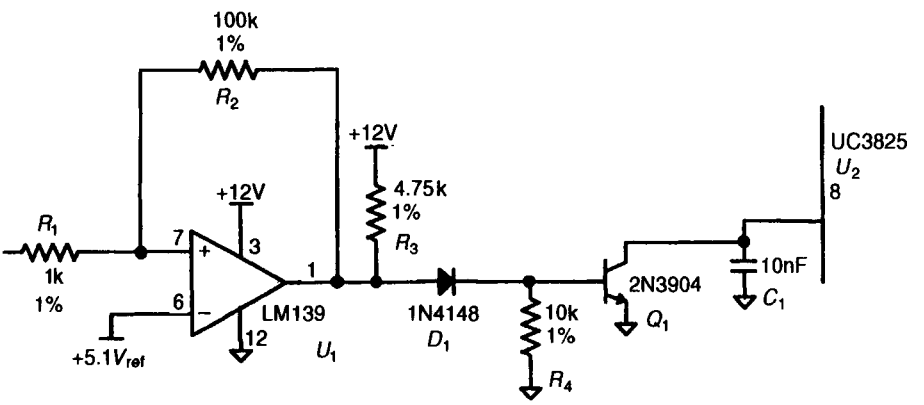

Figure 10.1 The circuit to be worst-case-analyzed is an overcurrent limit that shuts down the PWM.

You may observe that the output of the comparator does not go directly into the base of the BJT; rather, it passes through a dropping diode, which then requires a base turnoff resistor for the BJT. This is a necessary addition that will become clear as the WCA is performed; it was added to the schematic based on prior experience so that in the example, we won't have to go back, add it in, and re-analyze the system.

Properties to Be Analyzed

Having decided on the circuit function to be analyzed, we must consider what properties to analyze. Generically, we want to analyze the circuitry that responds to the input, that which generates the output, and any other circuits that interface between the two; some engineering judgment is necessary to select the important functions in a circuit. For this example:

1. We'll want to know the level at which the comparator trips on in response to an overcurrent, both minimum and maximum (but not where it comes back off, at least not for this example analysis).
2. We'll want to verify that the transistor is indeed normally off (if the output saturation voltage of the comparator is too high, the BJT might be always on).
3. We'll want to know how long the BJT will take to discharge the capacitor, turning off the PWM, given the transistor's limited beta.

In a more complete analysis, we might also want to check the maximum collector current on the BJT, to verify that it isn't going to be overstressed when discharging the cap, since it has no limiting resistor and may have a high beta.

We also need to know the conditions under which the circuit is going to operate: assume minimum temperature of $-40°C$ and a maximum of $+85°C$.

The next step is to develop a table listing the worst-case values of all the relevant parameters. In practice, you'd take a guess at the parameters needed, adding more items as the analysis progressed, or occasionally deleting some that proved to be unnecessary. Table 10.1 displays the final product.

Table Evaluation Techniques

Let's examine Table 10.1 closely. The first thing to observe is the column headings. Of course there is a part type column to identify each component's nominal value. Next is a column for a reference designator; there might be more than one type of 1kΩ resistor (e.g., to accommodate different temperature coefficients). The next column defines the parameters to be examined, such as the output saturation voltage of a comparator, the limit in which it's to be examined (minimum or maximum), and the conditions under which the limit is to be taken, such as the collector current at which the voltage is measured. Next come columns for the initial value (meaning nominal value at room temperature), initial tolerance (i.e., manufacturing tolerance), and temperature coefficient. In some circumstances, additional columns might be needed to display factors for age or radiation effects. Wedged in between are two columns labeled "Scale type" and "Scale factor." These are for additional factors that allow us to work around the limitations of data sheets. Thus if we need to know the output saturation voltage of the comparator at 2.5mA but the data sheet has a printed *value* only at 4mA and then a *curve* showing a scaling factor, we would go to the scale type column for an explanation of the scaling factor; we would put an evaluation in the scale factor column. Finally, there are columns for the two temperature extremes, since the results of the calculation are not symmetrically distributed around 25°C: $-\Delta T = (25°C) - (-40°C) = 65°C$, while $+\Delta T = (85°C) - (25°C) = 60°C$.

The actual evaluation of some of the entries in Table 10.1 can require specialized techniques. To start with, observe that the entries are all done in worst-case: the minimum resistance is found by *multiplying* the 1% tolerance and the (50ppm/°C × 65°C) = 0.325% temperature coefficient, not adding them. Specifically, *don't* take 10kΩ × 99% = 9900Ω, and then 10kΩ × 99.675% = 9967.5Ω, with the total then assumed somehow to be a combination of these two. Rather, take 10kΩ × 99% = 9900Ω, and then 9900Ω × 99.675% = 9867.8Ω (rounded off here to 9868Ω).

Observe also the way the temperature coefficients are handled. The resistor specification says only that the tempco of the resistor is ±50ppm/°C, not whether it is positive or negative with temperature. Thus we must assume that the tempco is going to conspire to be either positive for minimum resistance at temperatures below ambient (i.e., as it gets colder the resistance decreases further, making the minimum smaller) or negative at temperatures above ambient (i.e., as it gets hotter, the resistance also decreases further, again making the minimum smaller), and oppositely for maximum resistance. Of course, chances are this coefficient is either positive or negative, not both; but lacking additional information, you have to assume the worst. Generally, an analysis will simply take the

TABLE 10.1 Listing of Worst-Case Values for Example Circuit

Part	Reference designator	Parameter	Initial value	Initial tolerance	Scale type	Scale factor	Temperature coefficient	At −40°C	At +85°C
1kΩ	R1	R, min	1,000Ω	1%			±50ppm/°C	986Ω	987Ω
1kΩ	R1	R, max	1,000Ω	1%			±50ppm/°C	1,013Ω	1,013Ω
4.75kΩ	R3	R, min	4,750Ω	1%			±50ppm/°C	4,687Ω	4,688Ω
4.75kΩ	R3	R, max	4,750Ω	1%			±50ppm/°C	4,813Ω	4,812Ω
10kΩ	R4	R, min	10,000Ω	1%			±50ppm/°C	9,868Ω	9,870Ω
10kΩ	R4	R, max	10,000Ω	1%			±50ppm/°C	10,133Ω	10,130Ω
100kΩ	R2	R, min	100,000Ω	1%			±50ppm/°C	98,680Ω	98,700Ω
100kΩ	R2	R, max	100,000Ω	1%			±50ppm/°C	101,330Ω	101,300Ω
10nF	C1	C, max	10nF	20%			+15%, −25%	13.8nF	13.8nF
1N4148	D1	V_f, max at 2mA	1V		I = 10mA → 2mA	0.88	1.28, 0.73	1.13V	642mV
2N3904	Q1	V_{be}, min at I_c = 1mA	650mV	0.87			−2mV/°C	696mV	446mV
2N3904	Q1	V_{be}, max at I_c = 50mA	950mV				−1, −1.1mV/°C	1.07V	940mV
2N3904	Q1	h_{fe}, min at I_c = 50mA	60				0.56, 1	34	60
LM139	U1	V_{ios}	5mV				4mV	4mV	9mV
LM139	U1	I_{ios}	25nA				75nA	100nA	100nA
LM139	U1	I_{ib}	100nA				200nA	300nA	300nA
LM139	U1	V_o, max at I_c = 2.5mA	400mV		I_o = 4mA → 2.5mA	0.62	300mA	430mV	430mV
UC2825	U2	V_{ref}, min	5.10V	50mV	Long term	25mV	0.4mV/°C	4.999V	5.049V
UC2825	U2	V_{ref}, max	5.10V	50mV	Long term	25mV	0.4mV/°C	5.249V	5.299V
UC2825	U2	I_{chrg}, max	9μA				11μA	20μA	20μA

worst value for each component, blithely ignoring whether the worst case occurs at cold temperatures for some components and at high temperature for others. Such inconsistencies usually turn out to be unimportant. In the rare case of an analysis that shows the circuit right on the borderline between meeting its requirements and not meeting them, one option is to do two worst-case analyses: one in which all values are taken at cold, and another taking all values at hot.

Dealing with scale factors is another interesting problem. Generally, the data sheet contains a curve of a parameter for *typical* data, not maximum (nor minimum). The proper method is to use the scale factor for the typical data *applied* to the worst-case data. For example, it will turn out that we will need to know the maximum output saturation voltage of the LM139 when it is drawing a current of 2.5mA. The data sheet gives a guaranteed maximum output saturation voltage at a current of 4mA of 400mV, so we need to scale the data to the lower current. A data sheet curve shows that the typical output voltage changes by a factor of 0.62 in going from 4mA to 2.5mA, and so the worst-case number is also scaled by the same factor. That is, the worst-case is 400mV × 0.62 = 248mV (for this factor). Making this table de novo, you might originally have simply used 4mA for the worst-case current. As the calculation progressed, you'd find through an iteration that the current is actually 2.5mA, and the table then could be adjusted as indicated.

It frequently happens that you are using a device with a temperature range wider than the one your device actually sees. Thus, the LM139 has data for −55°C and +125°C, even though we want only −40°C and +85°C. It is clearly reasonable to use the wider temperature data limits, since they certainly provide a bound on the actual temperature limits. In case of problems, it might be possible to look at a device in the same family with reduced temperature range—but this choice introduces some uncertainty (is it *really* the same?). Moreover, you'll often find no change in the data. The manufacturer is simply taking batches of devices and labeling them according to what tests they pass!

One more thing to pay attention to is the format used when the data sheet directly provides the worst-case number over temperature. For example, the LM139 I_{ib}, which is specified at room temperature as a maximum of 100nA, is specified over the temperature range considered as a maximum of 300nA. Rather than leaving the tempco column confusingly blank, it is better to pretend there is a temperature delta of 200nA, and use this in the data presentation to show why the answer is 300nA.

Finally, the part you are using may be underspecified. For example, an output electrolytic capacitor might not specify ESR at all, or specify it only at 60Hz.

Practical Note The best plan is to stay away from parts that are underspecified. Just because one sample worked in the lab, what makes you think the next one will be satisfactory? If you have to use such a part, it is safe to assume that the underspecified parameter is zero, or limited by another factor (e.g., power supply voltage). For the example of the electrolytic capacitor at the output of a power supply, assuming the ESR is zero will minimize the phase margin, clearly giving the worst case.

Worst-Case Analysis: Comparator Trip Levels

With the data tabulated, it is now possible to do the analyses, the first of which is to determine the voltage level at which the comparator will go from a low state to a high, both the minimum value and the maximum value. This information directly tells you, for example, the minimum current at which the circuit being monitored will function (so you know that it won't trip during normal operation) and the maximum current at which this circuit will start to function (so you don't pull so much current that something blows up). If the analysis reveals values that turn out to be unacceptable, you can go back and change the values and tolerances of the resistors, or possibly the type of comparator being used; the WCA of course shows which changes would be most effective.

Starting then with the minimum trip level, the minimum will occur for the minimum reference voltage from the PWM, which Table 10.1 lists as occurring at −40°C, 4.999V. Thus the comparator will certainly trip high or will have tripped high when the voltage at its noninverting terminal is 4.999V. Let's consider the factors that influence the voltage at this terminal. Foremost of course is the two resistors: the 1kΩ resistor forms a divider network for the input voltage with the 100kΩ, which goes to the output of the comparator. (Remember that comparator output is assumed to be low because the comparator hasn't yet tripped.) This output is not ground, though, because the comparator is sinking current from the 4.75kΩ resistor and thus has a saturation voltage. Additional factors are a potential offset voltage for the comparator, and its input bias and offset currents. Let's tote all these factors up into an equation:

$$\frac{V_{trip} + V_{os} - 4.999\text{V}}{1\text{k}\Omega} + I_{ib} + I_{ios} = \frac{4.999\text{V} - V_{sat}}{100\text{k}\Omega}$$

Here, V_{trip} is the voltage that is causing the transition; the other notations are obvious. This is just Kirchhoff's law, that all the currents into the node at the noninverting input of the comparator must sum to zero. Since we want to find the *minimum* trip level, the offsets are added on to the trip voltage; that is, they are subtracted from the amount of current that the tripping voltage has to supply. Exactly the opposite will be done when we calculate the maximum trip level. Remember that offsets don't have a sign: they can be either positive or negative. Here we are choosing the positive (maximum) because it makes for the minimum trip level. As for the resistor values, we can at once see that making the 1kΩ as small as possible makes V_{trip} small; and therefore making the 100kΩ large makes V_{trip} small, because it multiplies the other side. Substituting values from Table 10.1, we write

$$\frac{V_{trip} + 9\text{mV} - 4.999\text{V}}{986\Omega} + 300\text{nA} + 100\text{nA} = \frac{4.999\text{V} - 430\text{mV}}{101{,}330\Omega}$$

and solving, V_{trip}, min = 5.052V. These equations show what is meant by solving the problem "mathematically": setting up an equation that determines the parameter, determining which parameters should be minimized and which maximized, substituting values from a table of worst-case values, and then solving numerically, either with a calculator (in this simple case of one equation) or with a computer program (if there are several equations in several unknowns, as sometimes happens).

With this solution in hand, it is straightforward to see that the equation for the maximum trip level is the same, except with all the factors that were minima now maxima, and vice versa:

$$\frac{V_{trip} + 9\text{mV} - 5.299\text{V}}{1013\Omega} - 300\text{nA} - 100\text{nA} = \frac{5.299\text{V} - 0\text{V}}{98{,}680\Omega}$$

The only other differences involve the various offsets, which now have a polarity that hinders the tripping rather than helping, and the saturation voltage, which is now assumed to be 0V rather than maximum. (It can't be less than zero because the comparator has ground for its negative rail.) Solving, we have V_{trip}, max = 5.363V.

Conclusion. The trip level will certainly be between 5.052V and 5.363V. If this were the voltage across a current sense resistor, you could divide by the resistor's value (including its worst-case!) and come up with the current levels at which this comparator circuit would trip. Note that you certainly could not have guessed this answer, say by adding 2% tolerance to a 5.1V reference, and adding 1% for the resistors.

Worst-Case Analysis: The BJT Is Normally Off

The second analysis for the block of circuitry shown in Figure 10.1 is to verify that the BJT is off when the comparator is low. The (potential) problem is the comparator's output saturation voltage: after dropping through the diode, and sinking current into the 10kΩ base resistor, the voltage left should not be sufficient to turn on the BJT—otherwise, the converter could never start because the soft-start pin of the PWM was being held permanently low! In fact, precisely this can happen if the diode is not included in this circuit.

To make the calculations manageable (the actual characteristics of both the diode and the base–emitter junction are exponential, making complete equations transcendental), we can start by considering that the BJT is supposed to be off and verifying that this is a self-consistent solution. This means verifying that all the other components of the circuit, under the assumption that the BJT is off, in fact work in a way guaranteeing that it *is* off. This is a frequently used technique for dealing with discrete semiconductors. Although the results are the same as those found for writing out the full transcendental equation set, and then solving them numerically, the results are more humanly understandable—and therefore easier for a human to check. The author has seen commercially available numerical software that does not converge to the correct solution for problems of this sort.

To summarize the procedure before starting: we're going to find the maximum base–emitter voltage of the BJT when it's still off by putting the minimum listed collector current into the transistor, finding the corresponding base current by looking at the beta, and then observing that the V_{be} doesn't change as the collector current is decreased beyond this point, even to 0A. To get this V_{be} requires current through the base resistor; but this current comes through the diode, which has a forward voltage to conduct that much resistor current. The sum of the base–emitter drop and the V_f of the diode will be greater than the comparator's saturation voltage. Again: even to get "zero" collector current calls for some base–emitter voltage. But this requires current into the base resistor, and getting this current requires a diode drop, since the saturation voltage of the comparator isn't high enough to provide the base resistor with enough current to turn the transistor on.

The BJT's base current must thus by assumption be tiny. The smallest listed V_{be} in the data book is for $I_c = 1\text{mA}$, at which in worst-case $V_{be} = 446\text{mV}$. We can estimate the beta: guaranteed minimum at 25°C is 70; according to the data curves, 1mA corresponds to a normalized factor of 0.8. At −55°C, the normalization is 0.4, so the minimum $\beta = (70 \times 0.4/0.8) = 35$. The 1mA of collector current then corresponds to a base current of $1\text{mA}/35 = 29\mu\text{A}$. Furthermore, the curve for V_{be} versus I_c appears flat below $I_c = 1\text{mA}$, so as long as we're below the 446mV on the base, the transistor can be assumed to be off.

Now, to get 446mV on the base, we need a minimum current through the base resistor of $446\text{mV}/10\text{k}\Omega$, which is minimum when the 10kΩ is maximum: $I = 446\text{mV}/10{,}133\Omega = 44\mu\text{A}$. This current has to come through the diode. Now no manufacturer provides data specifying *minimum* forward voltage of a diode. Instead, the best we can do is to estimate a bound on the minimum V_f. Looking at the curves (which go down only to 100μA), at 100°C the $V_f = 300\text{mV}$. Since we are actually dealing with lower temperatures (and V_f increases with decreasing temperature), this is a good curve to choose for a minimum; tracing out the curve, it is clear that the V_f must be at least 200mV. So for the transistor to turn on, we need at least $446\text{mV} + 200\text{mV} = 646\text{mV}$. But since we already know that the maximum output saturation voltage of the comparator is 430mV, we know also that there is more than 200mV of margin to ensure that the transistor is off.

You can see what happens if the diode is not there: the margin is only $446\text{mV} - 430\text{mV} = 16\text{mV}$, and there might be enough inaccuracy in the base–emitter calculations to cause the BJT to turn on. This certainly would be the case if the 4.75kΩ pull-up were any smaller. So the diode and the base resistor do need to be there; in general, you just design all your "comparator driving base" circuits with the diode and base resistor. Then it's not necessary to repeat this calculation each time.

The conclusion is that the BJT stays off during normal operation.

Worst-Case Analysis: How Long Until the PWM Is Turned Off?

The final analysis done in this example is to determine the maximum amount of time the BJT might take to discharge the soft-start cap. Since this circuit is being used as a current limit, you don't want much delay till shutdown, when the overcurrent condition occurs. The result of this analysis might pass on to a worst-case thermal analysis, say, of the switching transistor, to ensure that it can take the overcurrent for the calculated time without blowing up. The BJT has limited drive current, and finite beta, so it will pull current from the capacitor at some maximum rate, which then will determine when the PWM is off: pin 8 has to be pulled down from its initial 5V to 0.5V to shut down.

We're going to start by ignoring the propagation delay of the comparator (typically, 300ns) and look only at the capacitor discharging current; at the end, the delay will be added in. Now we need to get the minimum base current. The current is set by the 12V supply (which we'll assume is ±5% from another WCA not presented here), the 4.75kΩ resistor, and the forward drops of the diode and the base–emitter junction:

$$I_{base} = \frac{12\text{V} - V_f - V_{be}}{4.75\text{k}\Omega} - \frac{V_{be}}{10\text{k}\Omega}$$

This is again Kirchhoff's law. Here, the current into the base resistor lessens the current available for the base. To find minimum base current, we take minimum 12V supply,

maximum diode drop and base–emitter drop, maximum limiting resistance, and minimum 10kΩ (choosing the 10kΩ to pull as much current away from the base as possible). Conveniently, maximizing V_{be} works in the correct direction for both terms, both increasing the current shunted away from the base and decreasing the current passing through the 10kΩ. If this had not been the case, we would have had to take the derivative of I_{base} with respect to V_{be}, and found out whether minimum or maximum V_{be} minimized I_{base}. (Here, $dI_{base}/dV_{be} < 0$, so we need maximum V_{be}.) We are assuming in Table 10.1 that the collector current will be approximately 50mA; this is just an estimate, but it will be justified a posteriori by the calculation; that is, we assume this value, and at the end that value will be derived, showing that it was a self-consistent assumption. Substituting values, we write

$$I_{base} = \frac{11.4\text{V} - 1.13\text{V} - 1.07\text{V}}{4813\Omega} - \frac{1.07\text{V}}{9868\Omega}$$

or I_{base}, min = 1.80mA.

Having the minimum base current, we can find minimum collector current by determining minimum h_{fe}. At 50mA of collector current, minimum beta is 34, which requires a base current of 50mA/34 = 1.47mA, quite close to the actual calculated minimum base current; this then justifies the assumption we made in estimating V_{be}.

So with a minimum beta of 34, the minimum collector current will be 1.80mA × 34 = 61mA. Now the capacitor is originally charged to the 5V reference and has to pull down to 0.5V. In equations, since $I = C(dV/dt)$ and $t = C(\Delta V/I)$, discharge time t will be maximum for maximum capacitance and minimum collector current, as we already know. One additional factor is that pin 8 is still sourcing current, and so this factor should also be maximum. The whole equation is:

$$t = \frac{C\Delta V}{I_C - I_{pin8}}$$

Substituting numbers, we have

$$t = \frac{13.8\text{nF}(5.299\text{V} - 0.5\text{V})}{61\text{mA} - 20\mu\text{A}}$$

and of course the pin 8 current is negligible. We end up with $t_{max} = 1.1\mu$s, surely fast enough. Adding the propagation delay gives 1.4μs, so this value doesn't affect the matter. The conclusion is that when the input pin to this circuit exceeds the limit, the PWM IC will be turned off quite quickly.

Stress Analysis

Having done all of the worst-case analysis, for completeness we'll now do a stress analysis. The goal of a stress analysis is to guarantee that in operation, no component will be overstressed; or better, that no component will have applied to it stresses that are too close to its ratings. If a part is operated right at its maximum rating, not only is it more likely to occasionally have its rating exceeded during a transient, but also its MTBF is greatly increased. A stress analysis reveals which parts are likely to have a large influence on the reliability of the design.

The stress analysis itself simply is a table listing the stresses each part in the circuit sees, compared with the rated limits for the part. The comparison is done as a percentage,

that is, stress = actual/rating. Some companies provide derating guidelines (e.g., "resistors shall dissipate no more than 70% of their rated power"). If such a list is not available, it is probably acceptable to take the following as a rule:

> **Practical Note** Steady-state stresses should not exceed 90% of the manufacturer's ratings, and transient stresses should not exceed 100% of the manufacturer's ratings.

The end result is a column in a table like Table 10.2, showing that each part passes.

The stresses to be analyzed can be taken to be those that affect the reliability of the part, such as in MIL-STD-217. You would naturally expect to see data on power in a resistor, voltage on a capacitor, forward current and reverse voltage for a diode, and so on. Not every parameter a manufacturer specifies needs to be analyzed, only those that relate to the survival of the part.

Let's examine Table 10.2. The first column lists the components, each repeated as many times as there are stresses. Thus the LM139 is repeated three times, once each for its supply voltage, differential voltage, and common mode voltage. Normally, there would also be a column to list reference designators (since, e.g., a block could have several 1kΩ resistors), but we haven't bothered to assign references in this example. The parameter examined is in the next column, followed by the rating of the part, from the manufacturer's data sheet.

The actual stress is calculated in column 4. For most parts in a design, it is adequate to estimate the stress, since this value will be far less than its rating. For example, it's not necessary to think very hard to see that since the circuit has a maximum of 12V, the power dissipated in the 100kΩ resistor can't be more than $(12V)^2/100k\Omega = 1.5mW$, which is far less than the part's rated 100mW; we therefore don't care about its actual operation. Similarly, the 10kΩ resistor can have only about 1V on it, since it is clamped by the base–emitter junction; we don't even bother to list microwatts—just call it 0 watt. On the other hand, for the 1kΩ resistor, we calculate that the maximum voltage on the comparator side is 5.299V, and since the other side can be 0V, the power in the resistor could be as high as $(5.299V)^2/986\Omega = 28mW$, where we have used the minimum resistance value to get maximum power. As already stated, stress = actual/rated, and every cell in the Pass

TABLE 10.2 Example Stress Analysis Table

Part value	Parameter	Rating	Actual stress	Stress (%)	Pass
1kΩ	P	100mW	28mW	28	Y
4.75kΩ	P	100mW	34mW	34	Y
10kΩ	P	100mW	0mW	0	Y
100kΩ	P	100mW	1.5mW	2	Y
10nF	V	50V	5V	10	Y
1N4148	I_f	200mA	3mA	1	Y
1N4148	V_r	100V	0V	0	Y
2N3904	V_{cco}	40V	5V	12	Y
2N3904	I_{ce}	200mA			
LM139	V_{cc}	36V	12V	33	Y
LM139	$V_{differential}$	V_{cc}	5V	42	Y
LM139	V_{cm}	V_{cc}	5V	42	Y

column should have a Yes. In some rare instances, a part doesn't in fact pass; this should be taken as a strong recommendation to substitute a part with a larger rating in the design, or give a satisfactory explanation for the failure.

The row for the maximum collector–emitter current in Table 10.2 hasn't been filled in because the analysis wasn't performed; we leave it to the reader to do this analysis, and decide whether the collector should in fact have a resistor to limit the current. In reaching this decision, it is probably acceptable to have an I_{ce} up to 400mA, since the 200mA is a DC rating, and BJTs can safely take double their rated current in a pulse (cf. Chapter 3). If this rule is adopted, an explanatory note at the end of the table would be needed.

Conclusions

The conclusions of the overall analysis of the circuit block are the results of each individual analysis: the comparator will trip between 5.052V and 5.363V; the BJT stays off when it's supposed to; the trip on overcurrent occurs in less than 2μs; and all parts are properly derated. Presumably these results could be checked against specifications, or, as indicated, passed on to the next WCA as input data.

SOME CONCLUDING THOUGHTS

As is evident from our detailed example, a fairly substantial amount of work goes into creating a WCA. However, there are no mysteries involved, just a lot of slogging through messy algebra. At the end of such an analysis, you can feel assured that the circuitry will work every time in production.

In general, given a good design at the start, very little circuitry has to be added to guarantee worst-case operation. By far the most common problems found in WCA entail values that must be be slightly adjusted. Occasionally a circuit will need some redesign, but experience in WCA will guide you in avoiding such designs from the beginning. There is thus usually not too much cost to production in assuring the circuit's good performance; the cost rather is up front in the designer's time, where it should be. WCA should be made a part of every design intended for production.