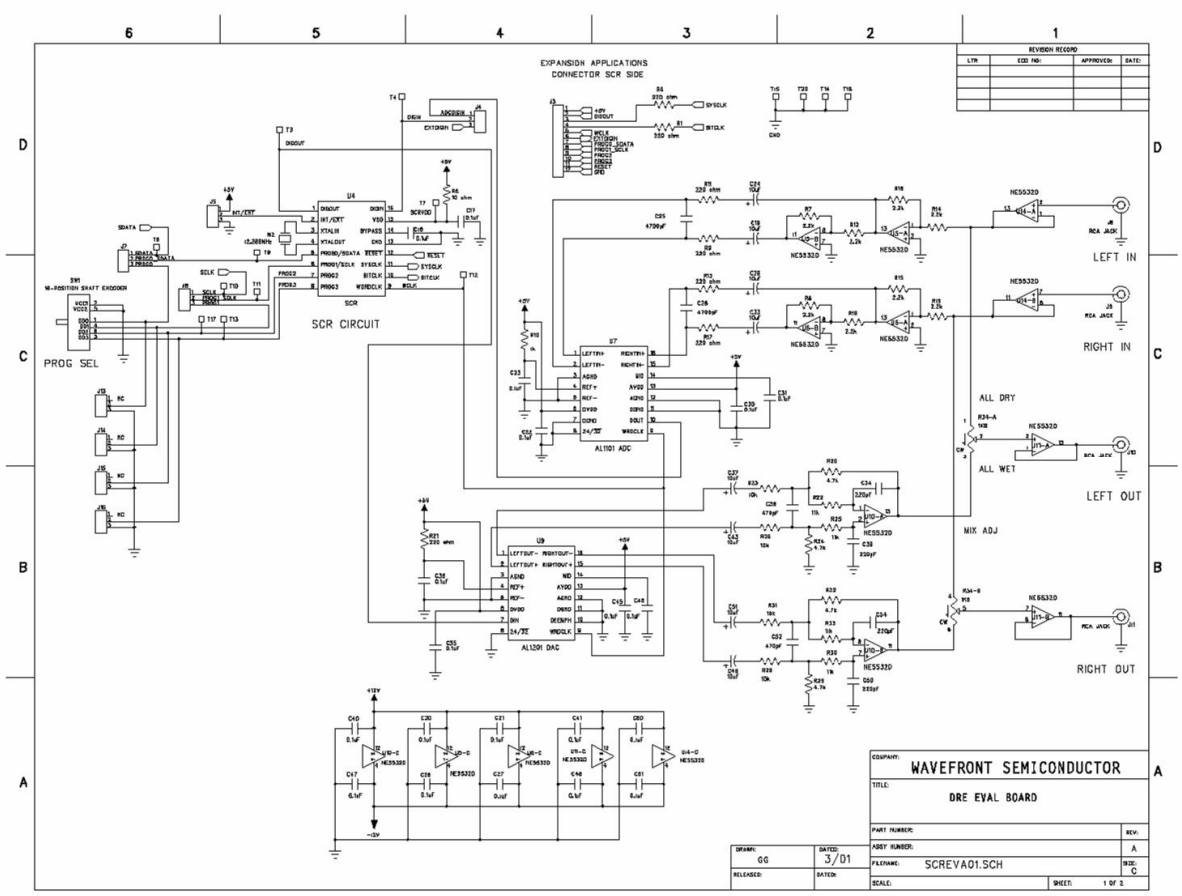
Evaluation Board for AL3201BG EV3201-A

General Description

The EV3201A provides an evaluation and development platform for the AL3201BG Digital Reverb Engine[1] IC. With the EV3201A, users can audition the internal reverb effects available on the AL3201BG or, using the supplied development software, develop and test custom reverb algorithms.

To assist with engineering design, an area on the board is set aside for additional circuitry the user may want to add, while expansion connectors are provided for system expansion.

In addition to the development software, the board is supplied with an AC adaptor and a serial interface cable.



1 Note that the AL3201B is referred to variously as the Digital Reverb Engine (DRE) and its older name, the Single-Chip Reverb (SCR).

Using the EV3201A

EV3201 POWER/GND CONNECTIONS

The AC input power jack for the EV3201A is at J2. A power supply "wall wart" is provided with the EV3201A (the country of origin should be specified when ordering. In most cases, Wavefront will be able to provide an appropriate power supply). DC voltages for the board are generated through on-board regulators. The required voltages are are +5VDC (can be monitored at T5), +12VDC (can be monitored at T6) and –12VDC (can be monitored at T2).

To use external DC supplies (when Wavefront cannot provide an appropriate country-specific power supply, for example, or when it is desirable to experiment with other supply voltages) remove or cut R2, R3, and/or R5 as needed, and feed an appropriate DC supply to the test points as shown below:

Nominal DC Supply	Resistor to cut	Test point to feed
+5VDC	R3	T5
+12VDC	R5	T6
-12VDC	R2	T2

T1 is provided as a ground reference from/to these DC sources.

T1, T14, T15, T18 and T20 are GND test points and can be used for oscilloscope or other test equipment ground connections. There is one ground on the board (see PCB layout section).

R6 is provided as a resistor to measure the current being supplied to the AL3201BG Use test point T7 to monitor the VDD of the AL3201B directly.

EV3201 AUDIO INPUT/OUTPUT CONNECTIONS

The Left and Right analog inputs are unbalanced RCA inputs, J6 for the Left channel and J9 for the Right channel. An 8Vpp signal at J6 or J9 is the maximum amplitude signal allowable before clipping occurs at the ADC.

The Left and Right analog outputs are unbalanced RCA outputs, J10 for the Left channel and J11 for the Right channel. An 8Vpp signal is the maximum amplitude output at J10 or J11.

Please note the comments about noise and the RS-232 cable in the next section.

RS-232 CONNECTION

J12 is used to connect the RS-232 cable to a computer running the supplied development software. The male side attaches to the EV3201A and the female side attaches to the computer's serial port.

The noise floor of the audio output may be poorly affected by the RS-232 cable creating a ground loop or corruption of the ground floor at low frequencies due to a noisy computer environment. We suggest evaluating the internal reverb effects with the RS-232 cable disconnected. If excessive noise appears at the outputs when evaluating user-developed algorithms, disconnect the RS-232 after the program is loaded to the DRE. Reconnect the cable as needed to reprogram the chip.

EXPANSION CONNECTORS

J1 and J3 are the expansion connectors. Most of the AL3201BGs are accessible through J3 (allowing the AL3201BGto accept serial inputs and outputs directly, for example) through J3. J1 allows the on-board microcontroller port pins to be accessed in an emulator environment.

RESET CIRCUITRY

S1 is the microcontroller and SCR reset switch. Depressing the switch will send a momentary reset pulse to the microcontroller and SCR.

DRE INTERFACE JUMPERS

J5 is the internal/serial mode select pin. Set to INT, the AL3201BGwill use its internal programs selectable by the 16-position encoder SW1. When J5 is set to INT, J7 and J8 should be set to PRG0 and PRG1. Set to \EXT, programs can be loaded into the DRE using the supplied development software. When J5 is set to \EXT, J7 and J8 should be set to SDATA and SCLK.

Use J4 to select the audio input to the DRE. Set to ADCDIGIN, the AL3201B will receive audio data from the RCA inputs and on-board ADC. Set to EXTDIGIN, the DRE will receive audio data from the expansion header J3.

EV3201 CIRCUIT LAYOUT

The EV3101A uses a two-layer PCB with ground as a continuous copper pour on the bottom of the PCB, a practice we recommend for new designs. A ground plane directly under the chip reduces any EMI emissions emanating from the chip. The PCB traces and components are split into a digital side and an analog side to keep high frequency digital traces away from sensitive analog traces. All 0.1uF bypass capacitors are placed as close as possible to the pins they are filtering. Surface mount 0.1 µF ceramic capacitors (type X7R) are used for bypassing, allowing placement as close as possible to the pins they are filtering. Electrolytic capacitors (10µF) are connected to the power lines.

External Devices

Data converters

Data conversion is provided by Wavefront's AL1101 ADC and AL1201 DAC. These components provide excellent 48kHz performance (-107dB dynamic range), and are available at pricing suitable for the musical instrument market. The use of these ICs also simplifies circuit layout because the Wavefront ADC and DAC derive all high speed clocks via high-quality on-chip PLL circuits (ClockEZ™ technology). As a result, only the 48kHz word-clock from the AL3201B need be supplied to each converter.

Micro-controller

The on-board micro-controller is an 87C51 custom programmed to work with the supplied development software. However, almost any micro-controller (PIC, etc.) can be used to program and control the DRE. Please refer to the interface and timing descriptions in the AL3201BGdatasheet for more information.

NOTICE

Wavefront Semiconductor reserves the right to make changes to their products or to discontinue any product or service without notice. All products are sold subject to terms and conditions of sale supplied at the time of order acknowledgement. Wavefront Semiconductor assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Information contained herein is only for illustration purposes and may vary depending upon a user's specific application. While the information in this publication has been carefully checked, no responsibility is assumed for inaccuracies.

Wavefront Semiconductor products are not designed for use in applications which involve potential risks of death, personal injury, or severe property or environmental damage or life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness.

All trademarks and registered trademarks are property of their respective owners.

Contact Information:

Wavefront Semiconductor
200 Scenic View Drive
Cumberland, RI 02864 U.S.A.
Tel: +1 401 658-3670
Fax: +1 401 658-3680
On the web at www.wavefrontsemi.com
Email: info@wavefrontsemi.com