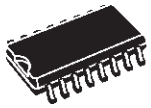
STPIC6C595

POWER LOGIC 8-BIT SHIFT REGISTER

- LOW $R_{DS(on)}$: 4Ω TYP
- 30mJ AVAILANCHE ENERGY
- EIGHT 100mA DMOS OUTPUTS
- 250mA CURRENT LIMIT CAPABILITY
- 33V OUTPUT CLAMP VOLTAGE
- DEVICE ARE CASCADABLE
- LOW POWER CONSUMPTION



SOP

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DESCRIPTION

This STPIC6C595 is a monolithic, medium-voltage, low current power 8-bit shift register designed for use in systems that require relatively moderate load power such as LEDs. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other low-current or medium-voltage loads.

The device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage register clock (SRCK) and the register clock (RCK), respectively. The device transfers data out the serial output (SER OUT) port on the rising edge of SRCK. The storage register transfers data to the output buffer when shift register clear (CLR) is high. When CLR is low, the input shift register is cleared. When output enable (G) is held high, all data in the output buffer is held low and all drain output are off. When G is held low, data from the storage register is transparent to the output buffer. When data in the output buffers is low, the DMOS transistor outputs are off. When data is high, the DMOS transistor outputs have sink-current capability. The SER OUT allows for cascading of the data from the shift register to additional devices.

Output are low-side, open-drain DMOS transistors with output ratings of 33V and 100mA continuous sink-current capability. Each output provides a 250 mA maximum current limit at T_C = 25°C. The current limit decreases as the junction temperature increases for additional device protection. The device also provides up to 1.5KV of ESD protection when tested using the human-body model and 200V machine model.

The STPIC6C595 is characterized for operation over the operating case temperature range of -40°C to 125°C.

ORDERING CODES

Type	Package	Comments
STPIC6C595M	SO-16 (Tube)	50parts per tube / 20tube per box
STPIC6C595MTR	SO-16 (Tape & Reel)	2500 parts per reel
STPIC6C595TTR	TSSOP16 (Tape & Reel)	2500 parts per reel

Figure 1 : Logic Symbol And Pin Configuration

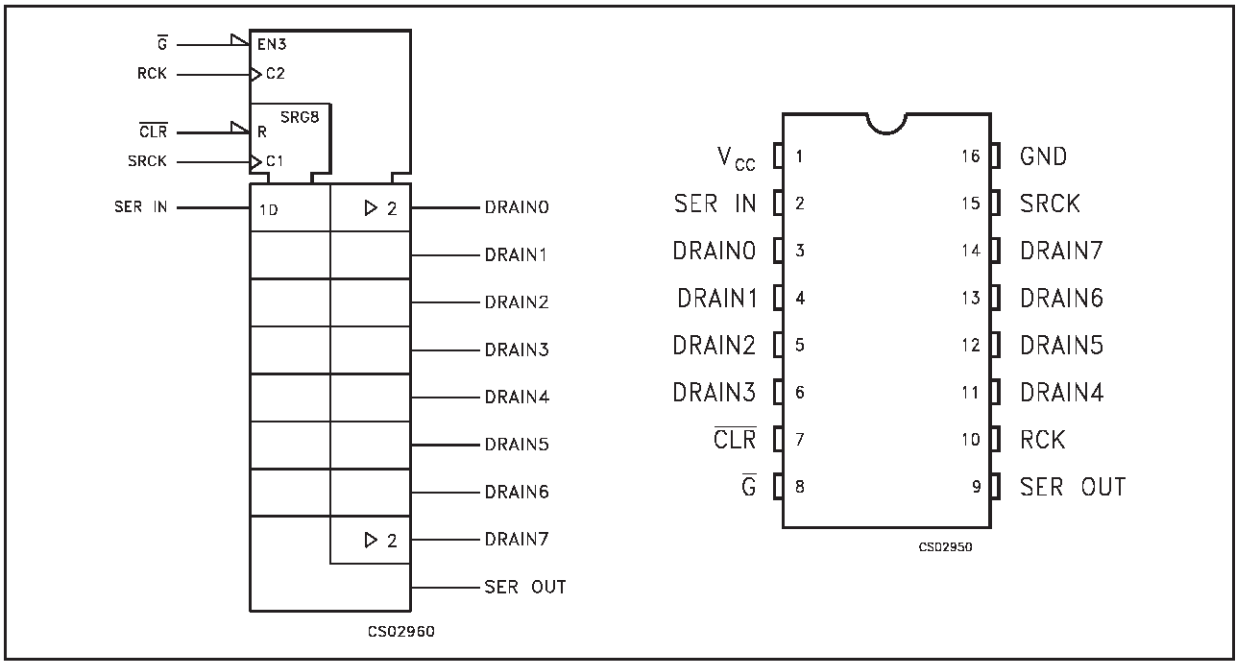
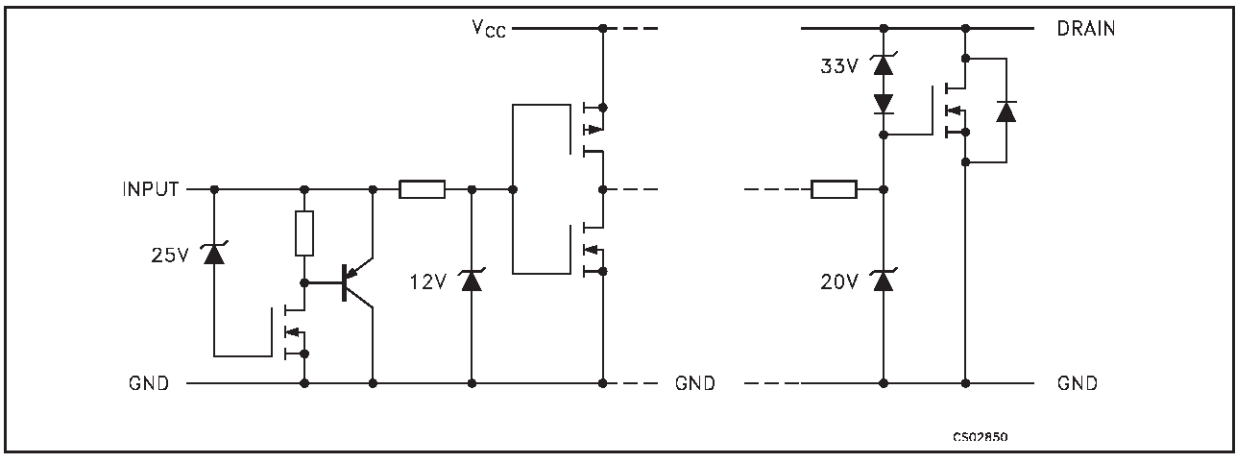


Figure 2 : Input And Output Equivalent Circuits



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Logic Supply Voltage (See Note 1)	7	V
V_I	Logic Input Voltage Range	-0.3 to 7	V
V_{DS}	Power DMOS Drain to Source Voltage (See Note 2)	33	V
I_{DS}	Continuous Source to Drain Diode Anode Current	250	mA
I_{DS}	Pulsed Source to Drain Diode Anode Current (See Note 3)	500	mA
I_D	Pulsed Drain Current, Each Output, All Output ON (T_C=25°C)	250	mA
I_D	Continuous Current, Each Output, All Output ON (T_C=25°C)	100	mA
I_D	Peak Drain Current Single Output (T_C=25°C) (See Note 3)	250	mA
E_{AS}	Single Pulse Avalanche Energy (See Figure11 and 12)	30	mJ
I_{AS}	Avalanche Current (See Note 4 and figure 17)	200	mA
P_d	Continuous total dissipation ($T_C \leq 25$°C)	1087	mW
P_d	Continuous total dissipation (T_C = 125°C)	217	mW
T_J	Operating Virtual Junction Temperature Range	-40 to +150	°C
T_C	Operating Case Temperature Range	-40 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature 1.6mm (1/16inch) from case for 10 seconds	260	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	115	°C/W

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Logic Supply Voltage	4.5	5.5	V
V_{IH}	High Level Input Voltage	$0.85V_{CC}$	V_{CC}	V
V_{IL}	Low Level Input Voltage	0	$0.15V_{CC}$	V
I_{DP}	Pulse Drain Output Current (T_C=25°C, V_{CC}=5V,all outputs ON) (see note 3, 5 and figure 15)		250	mA
t_{su}	Set-up Time, SER IN High Before SRCK ↑ (see Figure 6 and 8)	20		ns
t_h	Hold Time, SER IN High Before $\overline{G}$ ↑ (see Figure 6, 7, 8)	20		ns
t_W	Pulse Duration (see Figure 8)	40		ns
T_C	Operating Case Temperature	-40	125	°C

DC CHARACTERISTICS (V_{CC}=5V, T_C= 25°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSX}$	Drain-to-Source breakdown Voltage	I_D = 1mA	33	37		V
V_{SD}	Source-to-Drain Diode Forward Voltage	I_F = 100 mA		0.85	1.2	V
V_{OH}	High Level Output Voltage SER OUT	I_{OH} = -20 µA V_{CC} = 4.5V	4.4	4.49		V
		I_{OH} = -4 mA V_{CC} = 4.5V	4	4.2		V
V_{OL}	Low Level Output Voltage SER OUT	I_{OH} = 20 µA V_{CC} = 4.5V		0.005	0.1	V
		I_{OH} = 4 mA V_{CC} = 4.5V		0.3	0.5	V
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_I = V_{CC}			1	µA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_I = 0			-1	µA
I_{CC}	Logic Supply Current	V_{CC} = 5.5V All outputs OFF or ON		20	200	µA
$I_{CC(FRQ)}$	Logic Supply Current at Frequency	f_{SRCK} = 5MHz C_L = 30pF All outputs OFF (See Figg. 6, 18 and 19)		0.2	2	mA
I_N	Nominal Current	$V_{DS(on)}$ = 0.5V I_N = I_D T_C=85°C (See Note 5, 6, 7)		90		mA
I_{DSX}	Off-State Drain Current	V_{DS} = 30V V_{CC} = 5.5V		0.3	5	µA
		V_{DS} = 30V V_{CC} = 5.5V T_C=125°C		0.6	8	µA
$R_{DS(on)}$	Static Drain Source ON State Resistance (See Note 5, 6 and figg. 14, 16)	I_D = 50mA V_{CC} = 4.5V		4.5	6	Ω
		I_D = 50mA V_{CC} = 4.5V T_C=125°C		6.5	9	Ω
		I_D = 100mA V_{CC} = 4.5V		4.5	6	Ω

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_C= 25°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{PHL}	Propagation Dealy Time, High to Low Level Output from G	C_L = 30pF I_D = 75mA (See Figg. 4, 5, 6,7, 20)		80		ns
t_{PLH}	Propagation Dealy Time, Low to High Level Output from G			130		ns
t_r	Rise Time, Drain Output			60		ns
t_f	Fall Time, Drain Output			50		ns
t_{pd}	propagation Delay Time			20		ns
t_a	Reverse Recovery Current Rise Time	I_F = 100mA di/dt = 10A/µs (See Note 5, 6 and Fig. 9 and 10)		39		ns
t_{rr}	Reverse Recovery Time			115		ns

Note 1: All Voltage value are with respect to GND

Note 2: Each power DMOS source is internally connected to GND

Note 3: Pulse duration ≤ 100µs and duty cycle ≤ 2%

Note 4: Drain Supply Voltage = 15V, starting junction temperature (T_{JS}) = 25°C. L = 1.5H and I_{AS} = 200mA (See Fig. 11 and 12)

Note 5: Technique should limit T_J - T_C to 10°C maximum

Note 6: These parameters are measured with voltage sensing contacts separate from the current-carrying contacts.

Note 7: Nominal Current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5V at T_C = 85°C.

Figure 3 : Logic Diagram

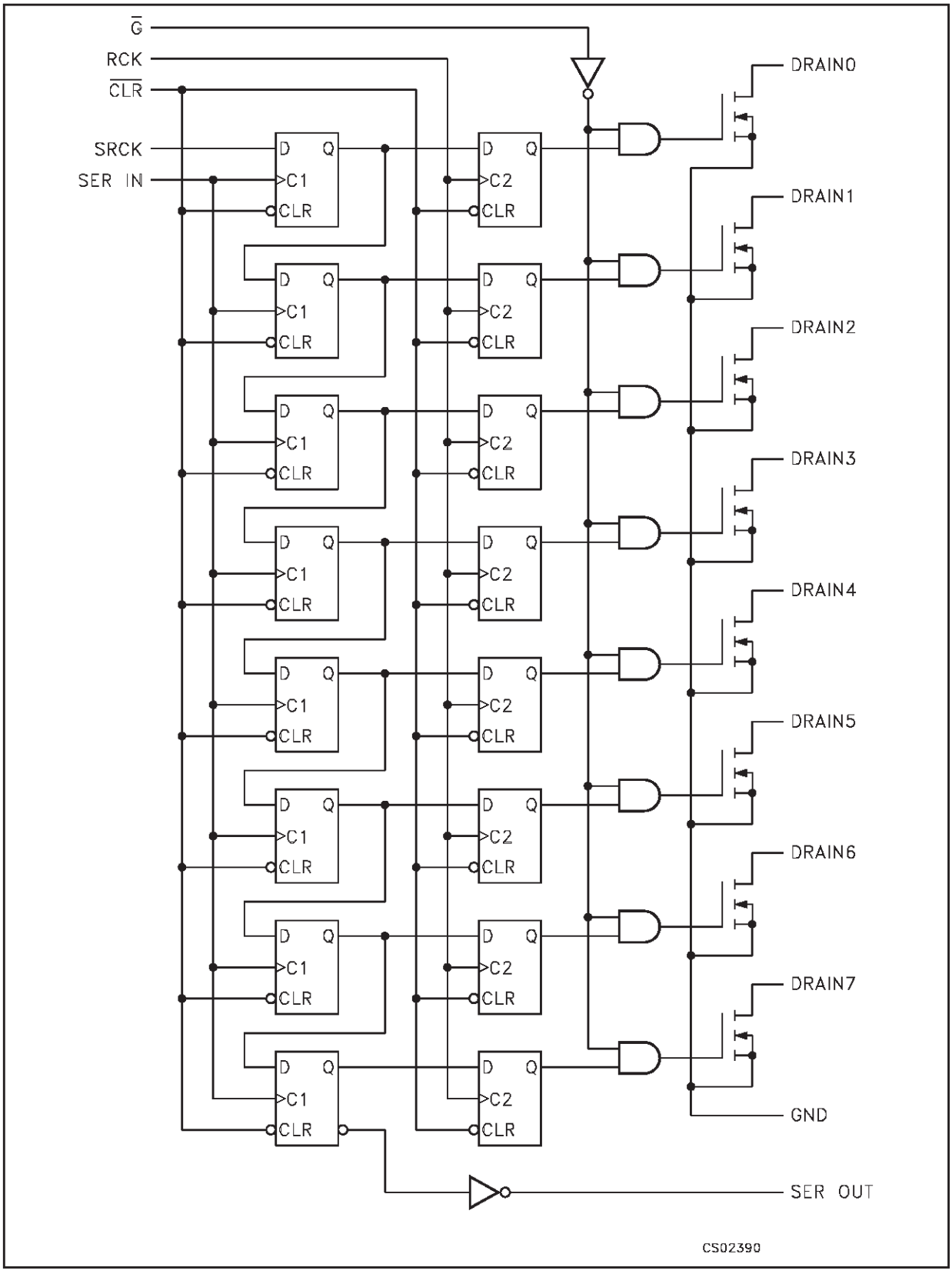


Figure 4 : Typical Operation Mode Test Circuits

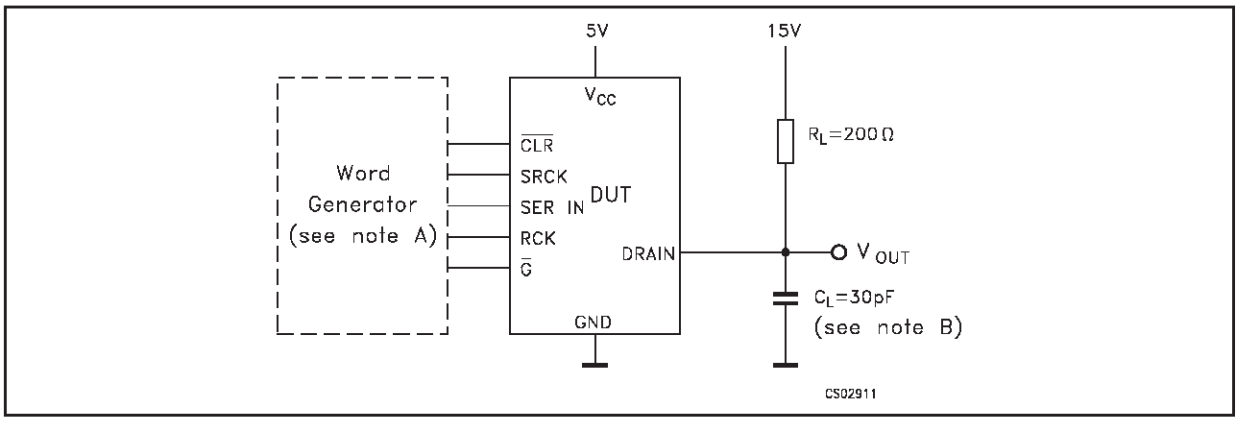
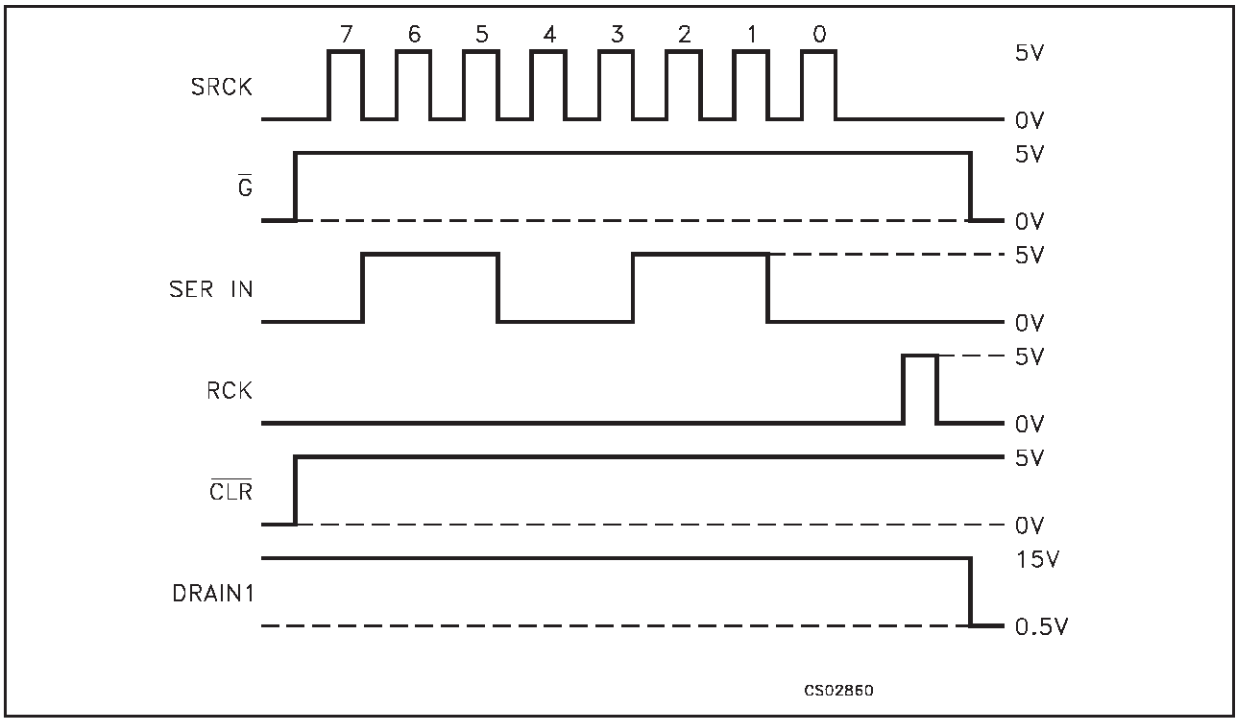


Figure 5 : Typical Operation Mode Waveforms



NOTE:
A) The word generator has the following characteristics: $t_r \leq 10ns$, $t_f \leq 10ns$, $t_W = 300ns$, pulse repetition rate (PRR) = 5KHz, $Z_O = 50\Omega$
B) C_L includes probe and jig capacitance.

Figure 6 : Typical Operation Mode Test Circuits

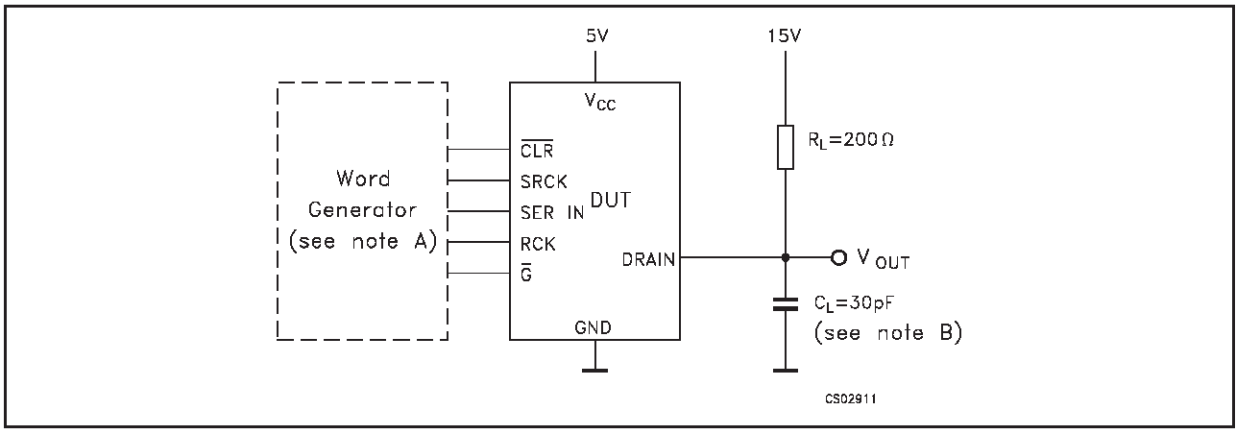


Figure 7 : Switching Time Waveform

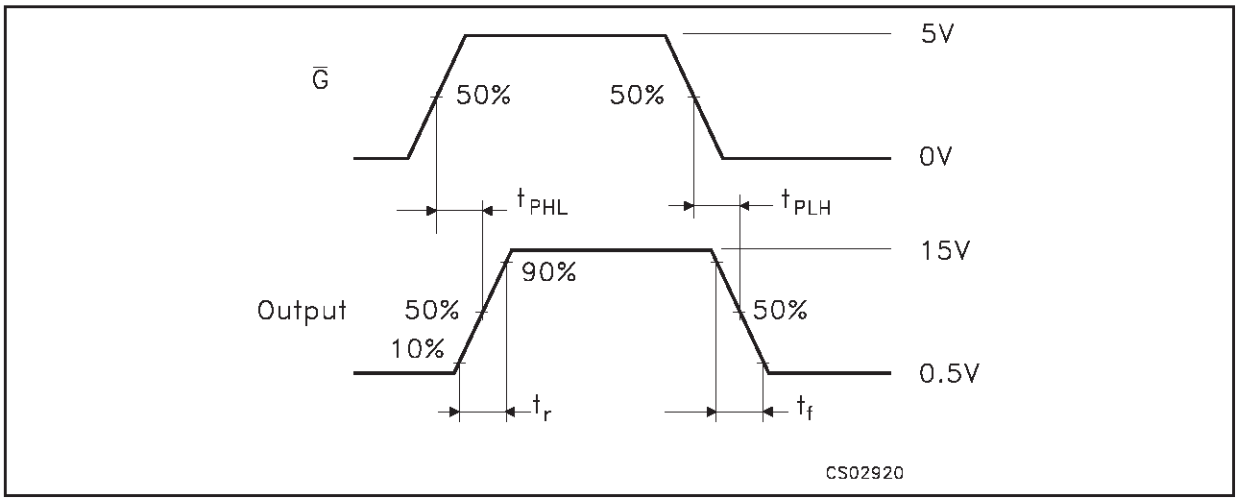
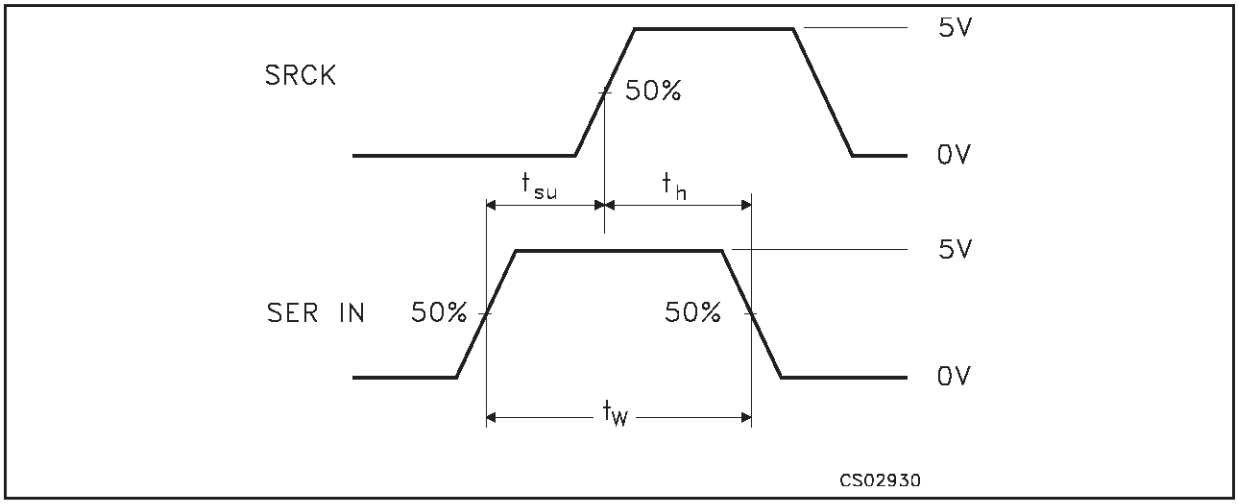


Figure 8 : Input Setup And Hold Waveform



NOTE:
A) The word generator has the following characteristics: $t_r \leq 10ns$, $t_f \leq 10ns$, $t_W = 300ns$, pulse repetition rate (PRR) = 5KHz, $Z_O = 50\Omega$
B) C_L includes probe and jig capacitance.

Figure 9 : Reverse Recovery Current Test Circuits

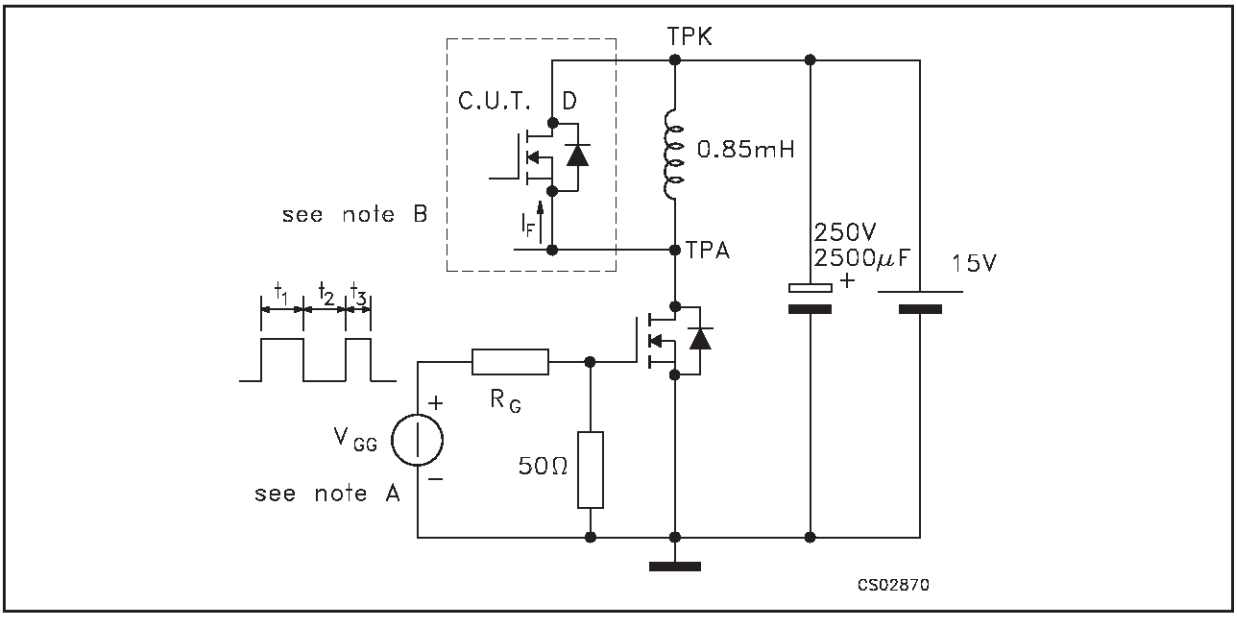
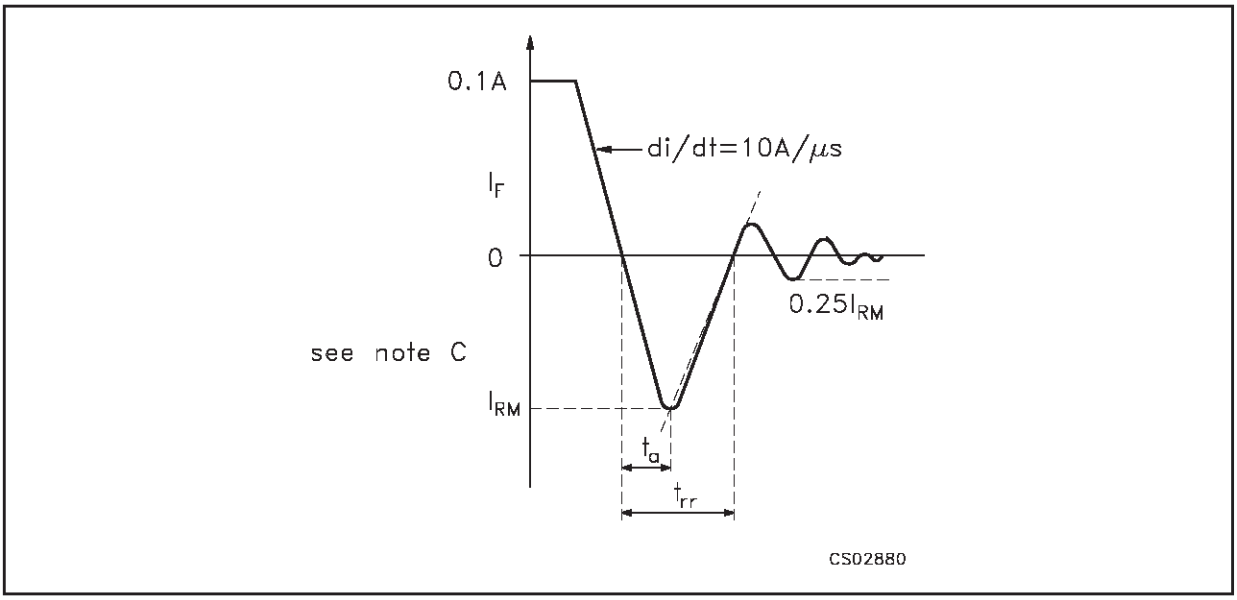


Figure 10 : Source Drain Diode Waveform



NOTE:
A) The V_{GG} amplitude and R_G are adjusted for di/dt = 10A/µs. A V_{GG} double-pulse trainn is used to set I_F = 0.1A. where t_1 = 10µs, t_2 = 7µs and t_3 = 3µs
B) The Drain terminal under test is connected to the TPK test point. All other terminals are connected together and connected to the TPA test point.
C) I_{RM} = maximum recovery current.

Figure 11 : Single Pulse Avalanche Energy Test Circuits

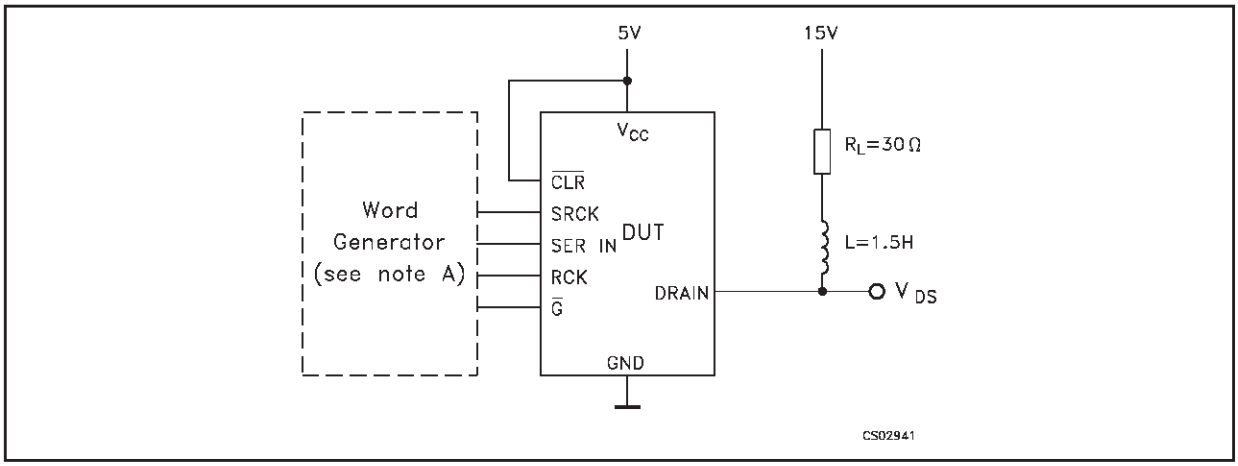
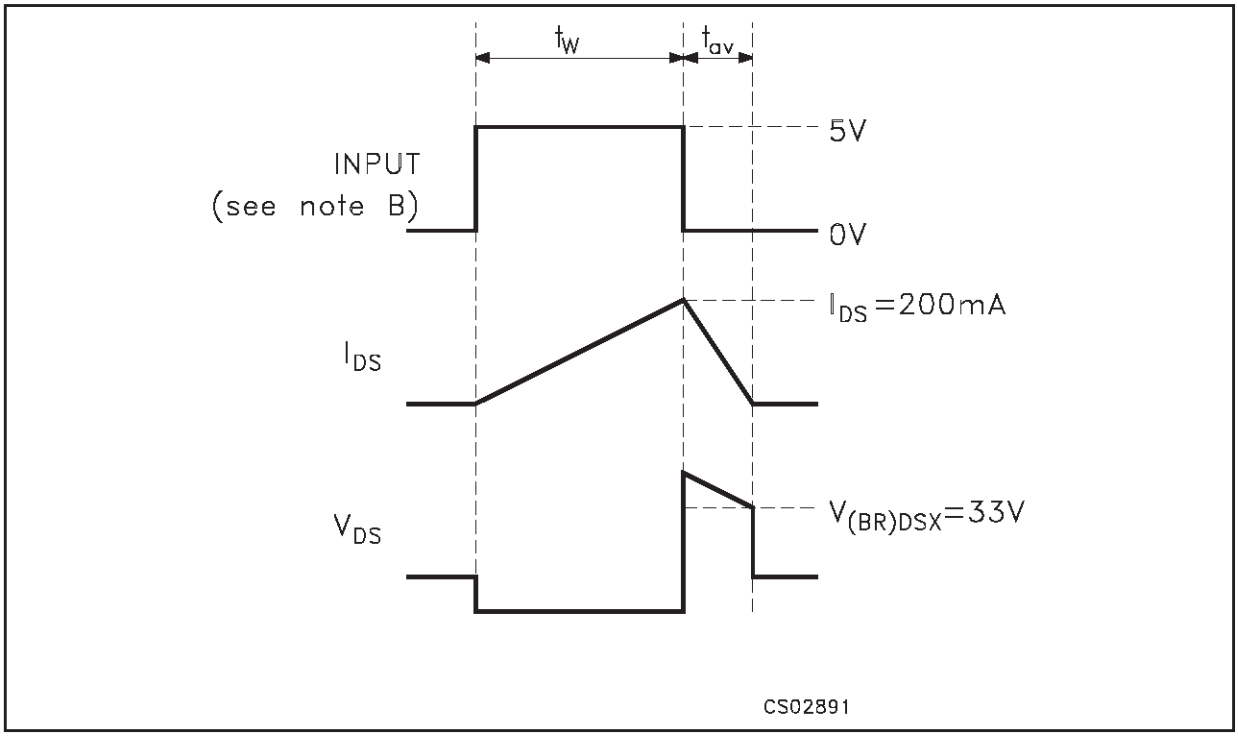


Figure 12 : Single Pulse Avalanche Energy Waveform



NOTE:
A) The word generator has the following characteristics: $t_r \leq 10ns$, $t_f \leq 10ns$, $Z_O = 50\Omega$
B) Input pulse duration, tW is increased until peak current I_{AS} = 200 mA. Energy test level is defined as $E_{AS} = (I_{AS} \times V_{(BR)DSX} \times t_{AV})/2 = 30mJ$.

TYPICAL PERFORMANCE CHARACTERISTICS (unless otherwise specified T_j = 25°C)

Figure 13 : Max Continuous Drain Current vs Number of Outputs Conducting Simultaneously

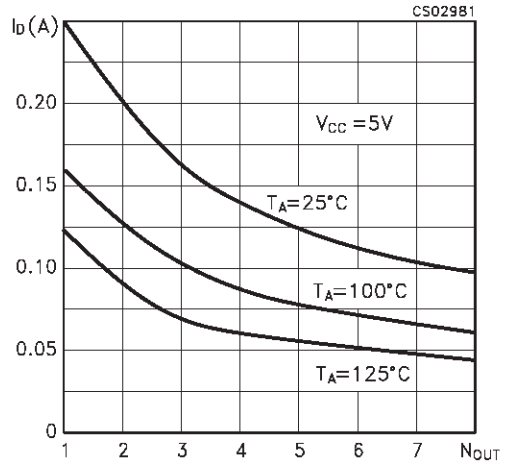


Figure 14 : Static Drain-Source ON-State Resistance vs Drain Current

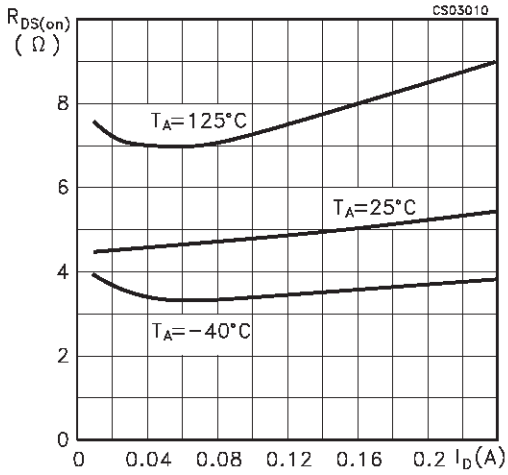


Figure 15 : Maximum Peak Drain Current vs Number of Outputs Conducting Simultaneously

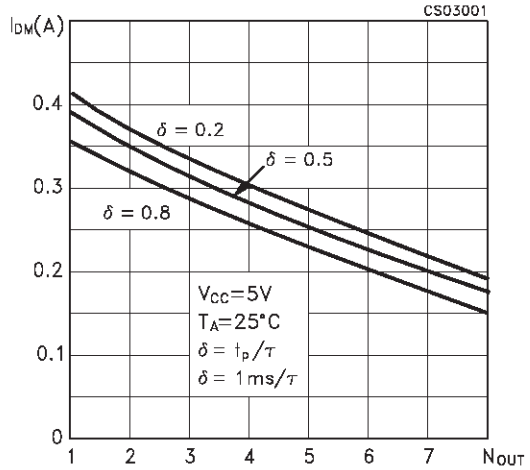


Figure 16 : Static Drain-Source ON-State Resistance vs Logic Supply Voltage

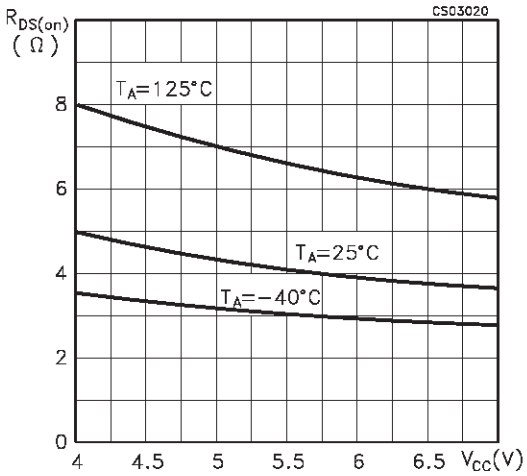


Figure 17 : Peak Avalanche Current vs Time Duration of Avalanche

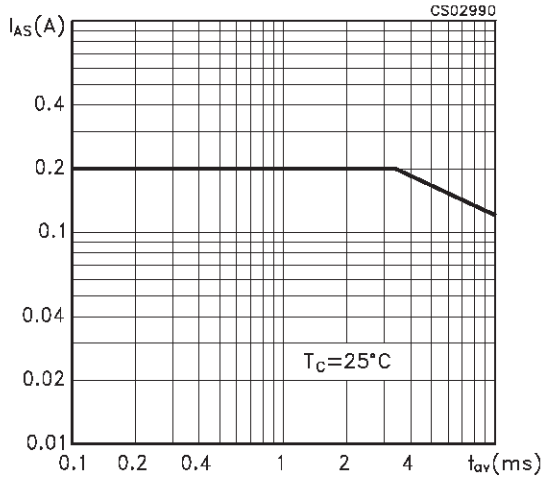


Figure 18 : Supply Current vs Frequency

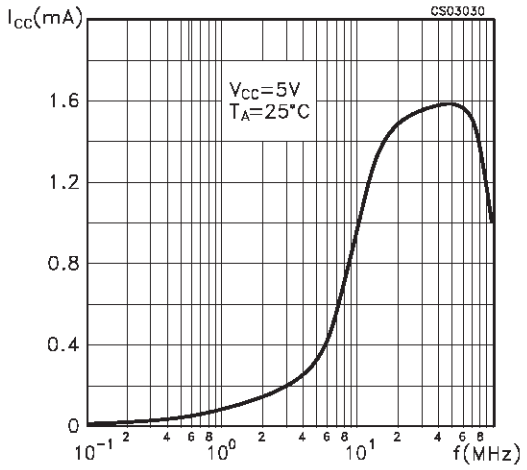


Figure 19 : Supply Current vs Supply Voltage

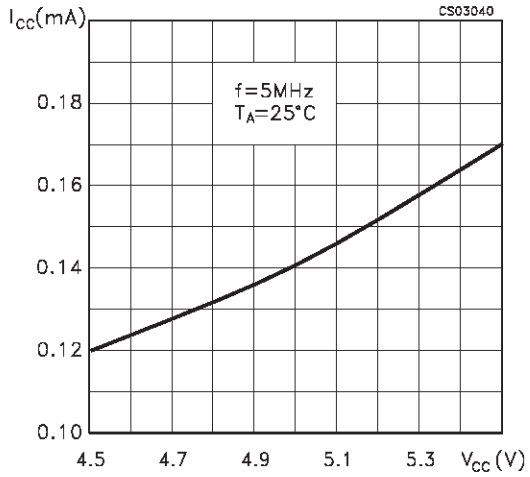


Figure 20 : Switching Time vs Case Temperature

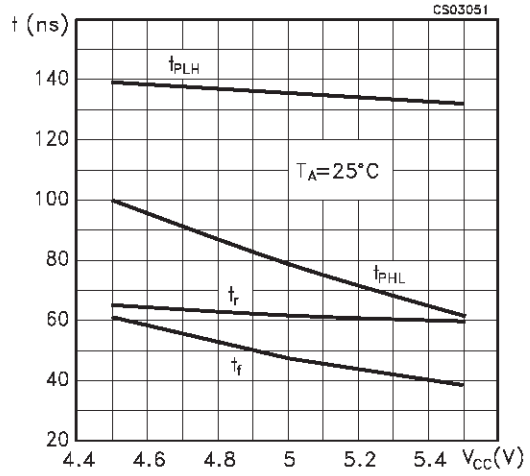
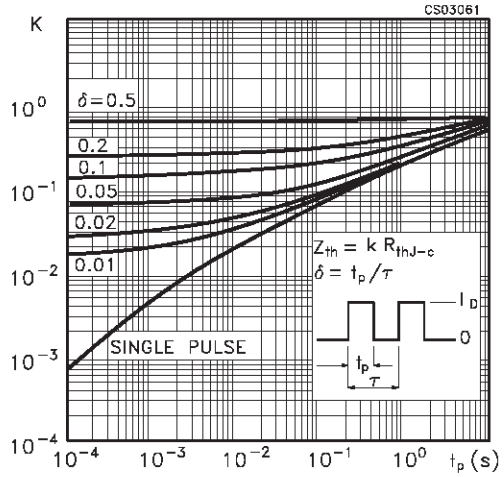
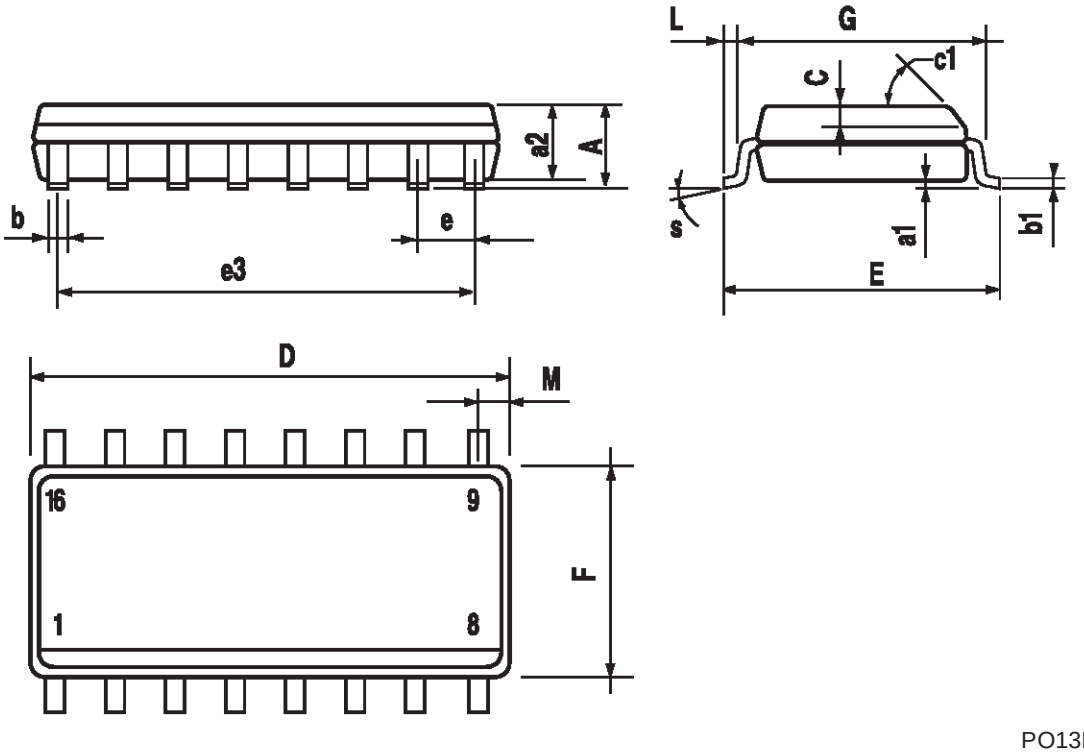


Figure 21 : Normalized Junction to Ambient Thermal Resistance



SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030